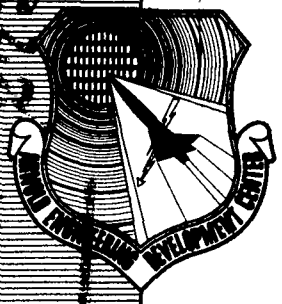
AEDC-TDR-62-61



A HIGH-SPEED, SOLID-STATE, DIGITAL SCANNER FOR USE WITH THE ERA 1102 COMPUTER

By

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ARNOLD ENGINEERING DEVELOPMENT CENTER
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE

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ABSTRACT

A high-speed, solid-state, digital scanner for entering data into the raw data system of the ERA 1102 computer is described. It was built for the PWT 16-Ft Supersonic Tunnel. The system capabilities, design considerations, theory of operation, and fabrication techniques are discussed.

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NOMENCLATURE

ERA	Engineering Research Associates Div., Remington Rand, Inc.
FF	Flip-flop
HSADC	High-speed analog-to-digital converter, Beckman 210 System
P^2B	Precision Pressure Balance system, Consolidated Electrodynamics Corp.
RDS	Raw data system for ERA 1102 computer
SLD	Shaper-line driver
SS	Single-shot multivibrator

1.0 INTRODUCTION

In the past a relay-type scanner has been used for commutating digital data from a number of shaft position digitizers and other analog-to-digital converters into the ERA 1102 digital computer. The shortcomings of such a system are obvious:

1. Limited speed
2. Wear of mechanical parts
3. Periodic maintenance required to clean contacts

Since modern digitizers are of an all electronic nature and, therefore, of higher speed, the limited speed of a relay-type scanner is much more apparent. Because a solid-state device to perform the scanning function in the 16-Ft Supersonic Tunnel of the Propulsion Wind Tunnel Facility, Arnold Engineering Development Center (AEDC), Air Force Systems Command (AFSC), could be built at a cost comparable to that of a relay scanner, the decision was made to construct such a device.

The scanner described is capable of scanning at any rate up to 15,000 channels per second. This will provide the capabilities of keeping abreast with modern data acquisition techniques. In addition, this scanner is wired for 24 binary digits per channel and 256 channels. Initial operation will be with 200 channels and 18 binary digits per channel. This provides three additional bits per channel over the relay-type scanner. The three extra bits will allow four binary-coded decimal digits plus two extra control or coding bits to be used.

At the present time the scanner will be operated at 20 channels per second in order to allow the present paper tape punch on the raw data system (RDS) to record the data simultaneously with entry into the computer. A magnetic tape recorder added to the RDS would allow higher speed operation. Should it be acceptable to bring the data into the computer without punching tape simultaneously, the speed of 15,000 channels per second can be realized. This mode of operation has been accomplished during the course of checking the scanner at 15,000 channels per second.

A typical example of scanning high-speed data would be the sampling of transient data by bringing it into drum storage at high speed, and if desired, punching it on paper tape on the high-speed output punch.

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Two internal loops are provided on the scanner. One provides for time-shared inputs from the Precision Pressure Balance system (P^2B) where 50 channels are scanned in a loop, and the other loop stops the scanner and allows several inputs to be brought in on one channel from the Beckman 210 System (HSADC).

Marginal checking techniques and simulated inputs with automatic checking circuitry have been incorporated into the design. An internal, variable speed, test oscillator allows checkout and maintenance of the scanner to be performed at the scanner location without the use of the computer.

2.0 DESIGN CONSIDERATIONS

2.1 BOOLEAN EXPRESSIONS

The Boolean expressions for a parallel word commutator of n channels and m bits per channel are:

$$B_1 = (C_1 \cdot B_{1-1}) + (C_2 \cdot B_{1-2}) + (C_3 \cdot B_{1-3}) + \cdots + (C_n \cdot B_{1-n}) \quad (1)$$

$$B_2 = (C_1 \cdot B_{2-1}) + (C_2 \cdot B_{2-2}) + (C_3 \cdot B_{2-3}) + \cdots + (C_n \cdot B_{2-n}) \quad (2)$$

$$B_m = (C_1 \cdot B_{m-1}) + (C_2 \cdot B_{m-2}) + (C_3 \cdot B_{m-3}) + \cdots + (C_n \cdot B_{m-n}) \quad (3)$$

where: $B_1 \ldots B_m$ are the commutated parallel bits

$C_1 \ldots C_n$ are enables, one each for the n channels to be commutated

$B_{1-1} \ldots B_{m-n}$ are the bits of the digital words to be commutated, i.e., B_{14-6} is the 14th bit of the word in channel 6.

The requirements for the commutator described are that $m = 24$ bits and $n = 256$ channels and that the 256 channels are to be commutated sequentially. This would suggest an 8-stage binary counter with an "And" matrix output to provide the C_1 through C_{256} sequential enables which are to be "And"ed with the various bits (B_{m-n}).

2.2 CHANNEL ENABLES

The Boolean expressions for the channel enables are:

$$C_1 = \bar{Q}_0 \cdot \bar{Q}_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3 \cdot \bar{Q}_4 \cdot \bar{Q}_5 \cdot \bar{Q}_6 \cdot \bar{Q}_7 \quad (4)$$

$$C_2 = Q_0 \cdot \bar{Q}_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3 \cdot \bar{Q}_4 \cdot \bar{Q}_5 \cdot \bar{Q}_6 \cdot \bar{Q}_7 \quad (5)$$

to

$$C_{256} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot Q_4 \cdot Q_5 \cdot Q_6 \cdot Q_7 \tag{6}$$

These can be grouped as follows:

$$C_1 = \left[(\bar{Q}_0 \cdot \bar{Q}_1)\right] \cdot \left[(\bar{Q}_2 \cdot \bar{Q}_3)\right] \cdot \left[(\bar{Q}_4 \cdot \bar{Q}_5)\right] \cdot \left[(\bar{Q}_6 \cdot \bar{Q}_7)\right] \tag{7}$$

$$C_2 = \left[(Q_0 \cdot \bar{Q}_1)\right] \cdot \left[(\bar{Q}_2 \cdot \bar{Q}_3)\right] \cdot \left[(\bar{Q}_4 \cdot \bar{Q}_5)\right] \cdot \left[(\bar{Q}_6 \cdot \bar{Q}_7)\right] \tag{8}$$

to

$$C_{256} = \left[(Q_0 \cdot Q_1)\right] \cdot \left[(Q_2 \cdot Q_3)\right] \cdot \left[(Q_4 \cdot Q_5)\right] \cdot \left[(Q_6 \cdot Q_7)\right] \tag{9}$$

which can be accomplished by obtaining the following 16 signals:

$$\begin{aligned}
&(\bar{Q}_0 \cdot \bar{Q}_1)(\bar{Q}_2 \cdot \bar{Q}_3)(\bar{Q}_4 \cdot \bar{Q}_5)(\bar{Q}_6 \cdot \bar{Q}_7) \\
&(Q_0 \cdot \bar{Q}_1)(Q_2 \cdot \bar{Q}_3)(Q_4 \cdot \bar{Q}_5)(Q_6 \cdot \bar{Q}_7) \\
&(\bar{Q}_0 \cdot Q_1)(\bar{Q}_2 \cdot Q_3)(\bar{Q}_4 \cdot Q_5)(\bar{Q}_6 \cdot Q_7) \\
&(Q_0 \cdot Q_1)(Q_2 \cdot Q_3)(Q_4 \cdot Q_5)(Q_6 \cdot Q_7)
\end{aligned} \tag{10}$$

where:

$\bar{Q}_0$ is the "0" output from the first stage of the 8-stage FF counter, Q_0 is the "1" output from the first stage FF to Q_7 which is the "1" output of the eighth FF.

2.3 2 x 2 MATRIX

These output functions (10) can be obtained by constructing four sets of 2 x 2 matrices. One of these sets using Q_0 and Q_1 takes the form of Fig. 1. From Fig. 1, obviously, the other three groups of enables can be obtained in the same manner.

2.4 4 x 4 MATRIX

It is now necessary to "And" the output of two of these small matrices together to obtain the terms in the first two brackets of Eqs. (7), (8), and (9). One of these matrices takes the form shown in Fig. 2.

Thus, there are 16 outputs from the first four FF's in the counter. These outputs would provide adequate enables for a 16-channel scanner.

In order to obtain the required 256 channel enables, it is necessary to build another matrix like that of Fig. 2, using Q_4, Q_5, Q_6, and Q_7 to obtain the terms in the second set of brackets in Eqs. (7), (8), and (9).

For simplification the matrix output has been given the symbols of:

$$\begin{aligned}
&\bar{Q}_0 \cdot \bar{Q}_1 = XXX0 \quad \bar{Q}_2 \cdot \bar{Q}_3 = XX0X \quad \bar{Q}_4 \cdot \bar{Q}_5 = X0XX \quad \bar{Q}_6 \cdot \bar{Q}_7 = 0XXX \\
&Q_0 \cdot \bar{Q}_1 = XXX1 \quad Q_2 \cdot \bar{Q}_3 = XX1X \quad Q_4 \cdot \bar{Q}_5 = X1XX \quad Q_6 \cdot \bar{Q}_7 = 1XXX \qquad (11) \\
&\bar{Q}_0 \cdot Q_1 = XXX2 \quad \bar{Q}_2 \cdot Q_3 = XX2X \quad \bar{Q}_4 \cdot Q_5 = X2XX \quad \bar{Q}_6 \cdot Q_7 = 2XXX \\
&Q_0 \cdot Q_1 = XXX3 \quad Q_2 \cdot Q_3 = XX3X \quad Q_4 \cdot Q_5 = X3XX \quad Q_6 \cdot Q_7 = 3XXX
\end{aligned}$$

Then XX13 would represent $Q_0 \cdot Q_1 \cdot Q_2 \cdot \bar{Q}_3$ which is one of the outputs from the first 4 x 4 matrix, Fig. 2.

2.5 16 x 16 MATRIX

The matrices described thus far are shown in detail on Dwg. 3201345-1. The outputs from the two 4 x 4 matrices must be used as inputs to a 16 x 16 matrix. From this the 256 required outputs are obtained and are shown in detail on Dwg. 3201345-2.

The matrices must be terminated through a resistor to a positive voltage to complete the "And" gates as shown in Fig. 3. The resistor (R_1) and the positive voltage (E_1) are determined by the desired rise time on the output wave form and the current which must be taken from the "And" gate. For minimum amplifiers the diodes used must have a low leakage current because of the number which are back-biased on any one line and must have a low forward voltage drop since, effectively, three are used in series. The diodes must also have adequate recovery time to run at the desired speed. 1N440 diodes were selected because of their relatively low cost and their very low leakage current. These silicon diodes were pre-tested for a leakage current of less than 0.1 microampere (μa) at 30 volts.

2.6 MATRIX SPEED

Examination of the diode matrix, Dwg. 3201345, sheets 1 and 2, will show that there are 38 diodes back-biased on any one line at a time.

At 6 pico-farads (pf) each for the 1N440 diodes biased in the reverse direction, this gives a total capacitance of 228 pf. Assuming a voltage of +50 volts, a resistance of 100K on the basis of the driving current required, and a desired output voltage swing of +25 volts, the voltage output from the matrix can be approximated with a step function input as follows:

Using $$e_{out} = f(t) = E\left[1 - \exp(t/RC)\right] \tag{12}$$

gives $$\frac{t}{RC} = 0.693$$

Assuming a total capacitance of 500 pf for diodes plus wiring capacitance and solving Eq. (12) for t, we obtain:

$$t = (0.693)(100K)(500) \times 10^{-12} \tag{13}$$

$$t = 34.7\ \mu\text{sec for the output enable to reach +25 volts}$$

or:

Maximum speed of $\frac{1}{34.7}\ \mu$sec = 28, 800 channels per second for the matrix alone.

The maximum speed at which the 1102 computer is capable of accepting information into drum storage is approximately 15, 000 channels per second.

2.7 MATRIX INPUT

There are 256 matrix resistors (R_i, Fig. 3) of 100K each to be driven from 16 FF sides; therefore, the load on each side can be calculated as follows:

$$R_i' = \frac{R_i}{256}(16) \tag{14}$$

$$R_i' = \frac{100K}{256}(16) = 6.25K$$

An emitter follower (Fig. 4) was used to isolate the FF's from the input to the matrix.

From Fig. 4, obviously, the transistor must draw approximately 4 ma to produce +25 v out. To produce zero volts output from the "And" gates approximately 8 ma are required. Maximum dissipation of the transistor occurs when the output is +25 v. This gives 100 mw (4 ma x 25 v) for collector dissipation.

2.8 MATRIX TERMINATION

The matrix output is terminated as shown in Fig. 5. The purpose of the diode, CR3, from the base to E_1 in Fig. 5 is to clamp the base circuit to 25 v maximum in case of circuit or power supply failure.

The beta (β) range on the 2N525 (T_1) is 30 to 64. With a beta of 30 the maximum base current required for saturation is:

$$I_b = \frac{E_1}{R_2(\beta)} \qquad (15)$$

$$I_b = \frac{35}{7.5\,K\,(30)} = 0.015 \text{ ma}$$

This imposes no problem for the "And" gate. Complete details of this circuit can be found on Dwg. 3201338 ("And-Or" gate driver type 9A1).

2.9 "AND-OR" GATE CIRCUITRY

Upon completion of the channel enables it is necessary to "and" these enables with the various bits to be commutated (B_{m-n}) (see Eq. (1)). This "And" gate must have an output to feed into an "Or" gate. The basic circuit is shown in Fig. 6.

The purpose of R_2 and E_3 (Fig. 6) is to hold the output down (to a "0") with the input contact open. The voltage divider formed by R_1 and R_2 from E_1 to E_3 must then be such that the voltage at this junction is less than zero volts under the worst margins of E_1 or E_2 expected. Twenty percent margins on one voltage at a time is a typical figure to which circuits of this type are normally designed. Best rise times are obtained with a high voltage termination on the "And" gate (E_1). Unfortunately, all current taken from the "And" gate must come through the resistor R_1 (Fig. 6). R_1 must then be small enough to keep the voltage drop through R_1 from exceeding the desired output voltage when current is taken from the "And" gate and yet must be large enough so that the two inputs to the "And" gate are capable of pulling the voltage down for the "0" condition.

If E_{out} is 25 volts for a "1", the maximum current which can be taken through R_1, for the output, is:

$$I_{R_1} = \frac{0.8\,E_1 - E_{out}}{R_1} = \frac{120 - 25}{620\,K} = 0.156 \text{ ma} \qquad (16)$$

With E_1 under its worst margin, 20 percent or 120 v, and the output voltage being +25 volts ("1"), then 0.156 ma is all that can be taken from the "And" gate.

Since there are 256 diodes on each "Or" gate the total leakage current of the diodes back-biased plus the input to the next stage must be very low. Type 1N440 silicon diodes were selected for the "Or" gate diodes because of their extremely low leakage current and relatively low cost. These diodes were selected to have a leakage current of less than 0.01 μa at -30 v at room temperature. Assuming all diodes in their worst condition, the total leakage current from these would be:

$$\text{Total leakage} = (\text{Number of "Or" gates} - 1)(\text{Leakage current per diode})$$
$$\text{Total leakage} = 255\ (0.1\ \mu\text{a}) = 25.5\ \mu\text{a} \tag{17}$$

Actually the leakage current will be much less than this since the diodes will only have -25 volts of bias, and the typical leakage current is 0.1 μa at -30 volts.

The maximum current required to keep the "And" gate down ("0"), zero volts out, under marginal condition is:

$$I_{R_1} \text{ in "0" condition} = \frac{1.2\ E_1 - E_{out}}{R_1} \tag{18}$$
$$I_{R_1} \quad \text{"0"} = \frac{1.2\ (150) - 0}{620\ \text{K}} = 0.29\ \text{ma}$$

Since each "And-Or" gate driver (Fig. 5) must drive 24 such "And" gates (Fig. 6), it must be capable of accepting 7 ma of current external to its emitter resistor:

$$I_{driver} = (\text{Number of bits per channel})\ (I_{R_1}\ \text{"0"})$$
$$= 24\ (0.29\ \text{ma}) = 7\ \text{ma} \tag{19}$$

The voltage divider formed by R_1 and R_2 (Fig. 6) with no input keeps the output down. This voltage under marginal conditions, neglecting the clamping from the channel enable with E_1 20 percent high, is:

$$E_{out(\text{Input contact open})\,n} = E_3 + [\,(1.2\ E_1 - E_3)\,]\ \frac{R_2}{R_1 + R_2}$$
$$= -30 + [\,1.2\ (150) + 30\,]\ \frac{100\ \text{K}}{(620\ \text{K} + 100\ \text{K})} \tag{20}$$
$$= -0.8\ \text{volts}$$

Assuming E_3 low (low negative) and $E_{out} = -0.1$ volt, the solution for E_3 is:

$$E_3 = -24.3 \text{ v}$$

a margin of 19 percent, which is considered adequate.

3.0 THEORY OF OPERATION

3.1 DIODE SCANNER CONTROL

3.1.1 Free-Running Multivibrator

The free-running multivibrator, Dwg. 3201330, is used as an internal clock source for checking purposes only. Its speed is continuously variable over the range of 20 channels per second to 20,000 per second in three ranges. Its output swing is about +30 volts, with the positive going edge used for operating the single-shot, 2K6 on Dwg. 3201343-1.

3.1.2 Clock Switching

Switching between clock sources is accomplished by SW1, SW2, and normal slave relay on Manual Selection Dwg. 3201344. SW1 selects either step clock pulse or the test multivibrator. Normal slave relay contacts 4 and 5 disconnect both of these test clock pulses when the normal relay is selected by the RDS.

SW2 selects either the regular read scanner pulse from the RDS or the test clock pulses. The function of SW2 is also bypassed by the normal slave relays, contacts 11 and 12.

3.1.3 Read Scanner Pulse

The read scanner signal is a 0.25 μsec pulse (SPB5) from a 3:1 pulse transformer in the RDS and is used to initiate all action in the scanner when under control of the RDS.

The read scanner pulse is coupled to the scanner through a pulse transformer with the primary side floating. This arrangement allows noise pulses picked up by the twisted pair transmission line to be cancelled and not be coupled to the scanner.

3.1.4 Single-Shot

The selected clock pulse from SW2 or normal slave relay goes to the SS 2K6A, Dwg. 3201343-1. The SS operates from the positive going edge of the pulse and has a 4-volt threshold bias on the input diode. The output pulse from the SS is negative going from +30 volts to ground and is about 5 μsec wide.

The leading edge of the input pulse must be sharp to obtain a sharp leading edge on the output. Poor wave form here will cause improper operation of the counter circuit.

3.1.5 Counter

The output from the SS, 2J13, Dwg. 3201343-1, is amplified by emitter follower 2J11 and samples the gates in 2K7 as well as the P^2B FF and HSADC FF. If gate 2K7-T is enabled, further amplification takes place in 2K9-B. Inverter 2J10-T and SS 2J13 re-shape the read pulse. The read scanner pulse samples the center input of all eight FF's in the counter (Q_0 - Q_7). An input on pin B of the FF's will cause the FF to toggle if pins M and H are enabled with +32 volts. If pin M only is enabled the FF will be cleared to a "0" by the center input pulse; with pin H only enabled, the center input pulse sets the FF to a "1". Q_0 is enabled at all times. Q_1 is enabled if Q_0 is a "1", Q_2 is enabled if Q_0 and Q_1 are "1"'s, and so on. Thus the "And" gates in 2J15 and 2J16 cause any specific FF to be set only when all lower order FF's are "1"'s.

Clear and set inputs are provided on the FF's for the use of the manual clear and set pushbuttons located on Panel 2J (see Dwg 3201344). Additional "Or" gates for setting the counter FF's are located on cards 2J17 and 2J18. The second set of "clear" and "set" lines are used for resetting the counter to the beginning of a loop and are controlled by the P^2B FF and gate 2K7.

3.1.6 P^2B Loop

The purpose of the P^2B FF is to reset the counter to a predetermined channel upon reading a certain channel. The channel upon which the counter is reset is controlled by the input to "And" gate 2K8-H which is patched to a channel enable through the plugboard. When the counter reaches the channel preceding which the counter is to be preset and the loop-scan contact is closed to +25 volts from the input equipment, the "And" gate 2K8 pins P and R are enabled, thus enabling the P^2B FF 2K11-H. The following read scanner pulse samples pin B of

this FF as it is advancing the counter one more count. The "0" output from the P^2B FF is then down, disabling the "And" gate and gate 2K7-T which prevents the counter advancing on the next read scanner pulse. This next pulse does pass through gate 2K7-U and is amplified (power-wise) in 2K9-T and resets the counter to a predetermined number through the plugboard. This same pulse clears the P^2B FF because pin M on the P^2B FF was enabled through the plugboard.

When the counter is to leave the P^2B loop the loop-scan relay from the input equipment is dropped, thus preventing "And" gate 2K8-P from being enabled and, consequently, any further action.

3.1.7 HSADC Loop

The operation of the HSADC loop is much the same as the P^2B loop except the counter remains on the channel on which it is stopped. On the channel before which the counter is to stop, the HSADC FF is enabled (2K10-H). The following read scanner pulse samples pin B and sets this FF, thus causing the "0" output to go down which drops the enable to gate 2K7-T through 2K8-M. This cuts off the advance of the counter and routes the read and advance HSADC pulse to the input equipment through the gate 2K7-D, emitter follower 2J11-B, inverter 2J10-C, single-shot 2J14-C, and emitter follower 2J19-B. 2K7-R is enabled from the plugboard by the channel enable on which the counter is stopped.

When the next to last channel in the HSADC loop is reached, a signal of +25 volts is received from the HSADC enabling 2K10-M. The gate 2K8-M is enabled, and the following read scanner pulse advances the counter and clears the HSADC FF, thus keeping 2K8-M enabled and operation of the counter is back to normal.

The signal from the HSADC for leaving the loop must appear with the data for the next to last channel in the HSADC loop only.

The read and advance HSADC pulse is a negative going pulse to -30 volts from ground with a 0.5-μsec leading edge and 30-μsec trailing edge and is about 5 μ sec wide at the -30 volt level. The pulse from gate 2K7-D is negative going from +25 volts and is inverted to a positive pulse in the inverter 2J10-C which operates the SS in 2J14, reshaping the read and advance HSADC pulse. SS2J14-C and emitter follower 2J19-B operate between ground and -30 volts.

3.1.8 Diode Matrix

The outputs from the eight counter FF's go to the 7A1 emitter followers in 2K9, 2K12, and 2K21. These emitter followers use the type 2N464 PNP transistor with 10K emitter resistors. Operation of the matrix has been explained previously in Section 2.5.

3.1.9 "And-Or" Gate Drivers

The output of the diode matrix is terminated into the "And-Or" gate drivers as explained in Section 2.5. The output of the "And-Or" gate drivers is patched to the "And-Or"gates through the plugboard, and thus the sequence of inputs is controlled. Two hundred and fifty-six outputs are available. Input connectors are associated with the physical location of the "And-Or" gates and not the "And-Or" gate drivers. Channel enable inputs must be patched to ground on the "And-Or" gates for the channels which do not have "And-Or" gate drivers patched in.

3.1.10 Input Requirements

The logic for the "And-Or" gates is shown in Dwg. 3201347. It takes four type 10A1 cards to constitute one channel of 24 bits. Input connectors are Amphenol, type #165-27, 24-pin, male receptacles located on the back side of the scanner in vertical rows (see Fig. 7).

For a "1" input, +25 to +35 volts must be developed across a 100K resistor returned to -30 volts and a 620K resistor returned to +150 volts. Under normal operating conditions, up to 0.35 ma would be required from a contact closure to +25 volts. For a "0" the digit input line must be left open or zero volts applied to the input terminal from a source capable of handling up to 0.058 ma. Exact current input requirements are a function of the input voltage and whether the input circuit is doing the major portion of the clamping to the "And-Or" gate or the word line driver input is doing the clamping. The output of a positive "And" gate is, of course, always the lowest voltage put into any of its "And" inputs.

For those who would care to check the input requirements for other than the cited examples, Fig. 8 is the equivalent circuit which should approximate the maximum input requirements, assuming normal operating voltages on the scanner and clamping being done by the input.

$$E_1 - E_s - I_1 (R_2 + R_3) + I_2 R_s = 0 \qquad (22)$$

$$- E_3 + E_s + I_1 R_s - I_2 (R_2 + R_s) = 0 \quad (23)$$

$$I_s = I_2 - I_1 \quad (24)$$

$$E_{in} = E_s - I_s R_s \quad (25)$$

$$E_{in} = 0 \text{ volts for "0" input} \quad (26)$$

$$+ 35 \text{ v} \geq E_{in} \geq + 25 \text{ v for "1" input} \quad (27)$$

3.1.11 "And-Or" Gate Operation

Inputs to the "And-Or" gates may be present at all times. No output results until the channel enable appears on the channel to be scanned. This enable is programmable through the plugboard as stated previously. When the channel enable and a "1" appear at the input to an "And" gate, an output appears into the "Or" gate shown in Fig. 6. The output of the "Or" gates is tied to a common bus line for the individual digits and is fed into an SLD for amplification. The common digit bus lines are spaced, and in no case laced together, in order to prevent cross-talk and excessive capacitance to ground since these are high impedance lines.

3.1.12 Shaper-Line Driver

The purpose of the SLD is to amplify, shape, and lower the impedance of the commutated bits for transmission to the RDS of the 1102 computer. These transmission lines are twisted pair, having an estimated characteristic impedance of 100 ohms and a distributed capacitance between the pair of 0.006 μf per 1000 ft.

The "Or" outputs of the "And-Or" gates are separated into two separate lines in order to reduce the total capacitance on these lines and thus increase the speed. These two lines go to the SLD card on pins F and T, Dwg. 3201351, and are amplified in the two 2N167 (Q_1 and Q_2) transistors. The output of these transistors are joined together in diodes CR3 and CR4. Transistor Q_3 gives additional amplification and presents a very low impedance source to +27 volts when a "1" is present. This output is fed to the output terminal pin E through diode CR5 which charges the line capacitance. Transistor Q_4 is an amplifier and provides the 180-deg phase shift necessary to drive Q_5. Q_5 is an emitter follower and provides a very low source impedance from the emitter to collector to -4 volts when a "0" is present. This output is coupled to pin E through diode CR6 which discharges the line capacitance.

The schematic of the SLD is shown on Dwg. 3201351 and the card location logic on Dwg. 3201348. Upon reaching the RDS the output from the SLD operates the suppressor grid of 7AK7 input gates through bias shifting networks.

3.1.13 Automatic Checking Circuitry

The hold-off voltage, E_3 (Fig. 6) is wired to the type 10A1 cards so that E_3 can be switched as follows:

1. -30 volts on all channels
2. +32 volts on odd-numbered channels and -30 volts on even-numbered channels
3. -30 volts on odd-numbered channels and +35 volts on even-numbered channels
4. +32 volts on all channels

This switching is done on the power control panel in rack No. 4. The switch is labeled sequentially 0-0, 0-1, 1-0, and 1-1. By switching to the 0-1 or 1-0 position, simulated inputs are obtained with alternate channels being all ones and all zeros. It is necessary that no input be present on the input connector to obtain this condition. When the "Normal" selection is made on the RDS the simulated inputs are disconnected by returning E_3 (Fig. 6) to -30 volts (see Dwg. 3201350 for switching diagram).

With the checking switch (SW3-2K), Dwg. 3201343-2, in the closed position, the master clear pulse samples the two inhibit gates 2J1-T and either sets or clears both Check I and Check II FF's depending on whether all ones or all zeros are to be read in on the first channel.

If the bit outputs of the channels being scanned are not all "1's" or all "0's" alternately, Check II FF will be toggled by the read scanner pulse, but Check I FF will not toggle because it will not be enabled. When Check I FF and Check II FF are not both in the same state, gate 2K7-T is not enabled by "And" gate 2K8, and thus stops the flow of read scanner pulses. The scanner will stop on the next channel after the one that has failed, and the failure can then be located.

3.1.14 Lamp Drivers

Indicator lamps were required on all FF's, and SLD's to allow the determination of the state of these circuits at a glance. At first, NE-2 neon lamps biased at -60 volts were used; however, the voltage

swing available for firing and extinguishing these lamps was +30 volts to 0 volts. Because of the inconsistent characteristics of neon lamps, some of them would not fire at 90 volts potential and some would not extinguish at 60 volts. Therefore, neon lamps were considered to be unreliable for these circuits. To provide reliable indicators, a lamp driver (16A1) circuit was designed that operates 24E, telephone-type, incandescent lamps. Four of these circuits are shown on Dwg. 3201397.

For analysis of operation, the circuit containing transistors Q_1 and Q_2 will be used. The outputs of the FF emitter followers and SLD's are used as inputs to this circuit. When the input is a "1", +30 volts is applied to R, resulting in the base of Q_1 becoming positive and saturating this transistor, producing a potential only slightly above ground at the collector of Q_1. This output is coupled to the base of Q_2, causing this transistor to also saturate and resulting in a positive potential of approximately 30 volts at the collector of Q_2. The output of the collector is externally connected to the 24E lamp that has its other terminal grounded. Thus, the lamp will turn on. When the input at R is near ground, both transistors are turned off because of the -10 v bias on Q_1 and the +45 v bias on Q_2, allowing no current to flow in the lamp.

4.0 FABRICATION

4.1 MECHANICAL

4.1.1 Card Chassis

The chassis or baskets for holding the printed circuit cards were fabricated at AEDC because no commercial chassis were then available that would fulfill the requirements. The chassis were built for mounting in 19-in. relay racks, with each one capable of holding 48 printed circuit cards. A 2.5-in. flange was provided on the left side to accommodate fuseholders, switches, and any control hardware required. Notched guide rails were provided at the top and bottom for each row of cards in order to allow the cards to be inserted in the connector with ease. The connectors were mounted on the chassis extending through cutouts. The connectors used were 18-contact Amphenol type 143-018-04.

4.1.2 Relay Racks

The card chassis were mounted in three Emcor Modular type 19-in. relay racks. A fourth rack was used to hold the power supplies for the system. Each rack has 78.75 in. of vertical space, allowing nine card

chassis to be mounted in each rack. Each rack was provided with a clear plexiglass door that allows observation of the operation with the doors closed. Figure 9 is a photograph of the racks before installation of the cards.

4.1.3 Plug Mounting Bracket

Brackets were fabricated by the PWT Machine Shop for holding the 256 data input connectors. These brackets were made from 0.1875 in. x 2.5 in. x 5.1875 in. extruded aluminum tees in lengths of 78.875 in. Two pieces were mounted in two racks, and one in the third rack. Each bracket holds 54 input connectors. Figure 7 shows the installation of the brackets.

4.1.4 Cooling System

The three racks that hold the printed circuit cards are each cooled by centrifugal blowers. Outside air enters through filters mounted in the rear doors and is directed through a false floor directly beneath the cards, passes through the cards, and exits through a grille at the top of the racks. No cooling air is provided for the power supply racks because the supplies are provided with their own cooling systems.

4.1.5 Printed Cards

The printed circuit cards were fabricated by the Technical Services Division, Instrument Branch, employing a commercial, copper-clad, laminated material. All cards were made 3.5 in. x 4 in. in size. Each type of card was keyed by sawing a slot in the card where there was an unused external connection. The connectors were keyed in the same manner to eliminate the possibility of a card being inserted in the wrong position. All components were mounted by hand-soldering. It was not economically feasible to use dip-soldering because of the limited number of cards to be fabricated.

4.2 ELECTRICAL

4.2.1 Color Codes

Each service voltage was assigned a color code, and this color of wire was used throughout the scanner for this voltage. Signal wires, except for data bit lines, were coded in accordance with their destination. For example, all wires destined for pin A on any connector were coded 41. Codes 01 through 24 were used for output bits 1-24 on the 10A1 ("And-Or" Gate) cards.

4.2.2 Chassis Wiring

In order to make chassis wiring easier, no direct wiring between relay racks was done. All signal wires running from rack to rack were wired to mating connectors mounted between the racks. All power distribution wiring was run to a common terminal strip. Before the chassis wiring was begun, all chassis were mounted in their racks. The racks were placed in a horizontal position on a work bench, allowing the wiring to become an easier task. When all racks were wired, they were interconnected using the connectors and terminal strips provided.

4.2.3 Power Distribution and Fuses

Power is distributed to the scanner from the power supply rack by relays that apply the power in a sequence that will not harm the components. The first relay applied +32, -10, and -60 volts. The second relay applies all other voltages an instant later. From the relay contacts the power goes to a group of terminal strips located in the center relay rack. From these terminal strips, power is distributed to the card chassis after passing through appropriate fuses. Fuses are located on the flange of the chassis provided for this purpose. All fuseholders are the indicating type.

4.2.4 Rack Interconnections

All interconnections of signal lines between the three racks of the scanner, excluding the power supply rack, pass through "Blue Ribbon" type connectors in order to allow the racks to be moved separately if the need should arise. In order to move the scanner, only the power supply lines and the input connectors would have to be removed.

4.2.5 External Connections

External connections to the scanner are of three types: control lines and bit lines to the RDS of the ERA 1102 computer, control lines to and from other pieces of input instrumentation equipment, and data inputs. The connections to the RDS are connected to terminal strips inside the scanner and proceed from there to telephone-type terminal blocks mounted in a junction box between the third and fourth rack. Permanent connections are provided from the terminal blocks to the RDS. Twisted pair is used for transmission. In some cases stray pickup on lines indicated that the twisted pair be allowed to "float" and be coupled to the scanner by pulse transformers. Coaxial cable was used to carry pulses to input equipment such as the HSADC and the P^2B system. Date input lines enter the scanner from cable trays on top of the racks and are terminated with 24-pin quick-disconnect connectors. Mating connectors are mounted on plug mounting brackets discussed in Section 4.0

4.2.6 Pre-Testing Components

The only components in the system that were pre-tested were the diodes. The 1N440 diodes were selected to have a leakage current of less than 0.1 μa with a reverse bias of 30 volts because of requirements discussed in Section 2.9. Figure 10 shows the circuit that was used.

Using this test arrangement all diodes were rejected that allowed a voltage drop across the 10K resistor greater than one mv. The rejection rate was very low. Only 2 percent of the diodes tested had reverse characteristics that did not meet requirements.

The reverse characteristics for the DR-292 diodes were not as critical as the 1N440. They were tested for reverse leakage current of no more than 30 μa at 30 volts. Approximately six percent were rejected on this basis.

4.2.7 System Checkout

The scanner was checked out in steps to insure that very few malfunctions would be encountered at one time. First, the counter and matrix were checked and wiring errors, bad components, and poor solder joints were removed. After the counter and matrix were operating properly, one channel of "And-Or" gates was plugged in at a time, and by using simulated bit inputs each bit was checked on each channel. At the same time, the bit output wave shapes were observed with an oscilloscope. At this point, it became apparent that the word line drivers (11A1 Cards) would not operate at high speeds with a large number of "And-Or" gates in the circuit. To correct this trouble, a new circuit was designed (15A1, shaper driver) to replace the word line drivers. After these circuits were installed, the automatic checking circuitry was added to the scanner. Using the simulated inputs of ones and zeros on alternate channels, the scanner was operated in conjunction with the RDS of the ERA 1102 computer. The system was operated constantly for several days in a continuous loop. After checking all of the tape punched by the RDS in this mode and investigating all failures, the end-scan circuit was added and several rolls of tape were punched using end-scan and automatic start. The final check using the RDS tape punch was in step-scan mode. The next step of the checkout was to run the scanner at a high rate of speed in the on-line mode without using the tape punch. Data were scanned from the HSADC and entered in computer storage by a minor, temporary modification of the RDS at a rate of 3000 channels per second. Also, utilizing the same RDS modification, simulated data were read into drum storage at

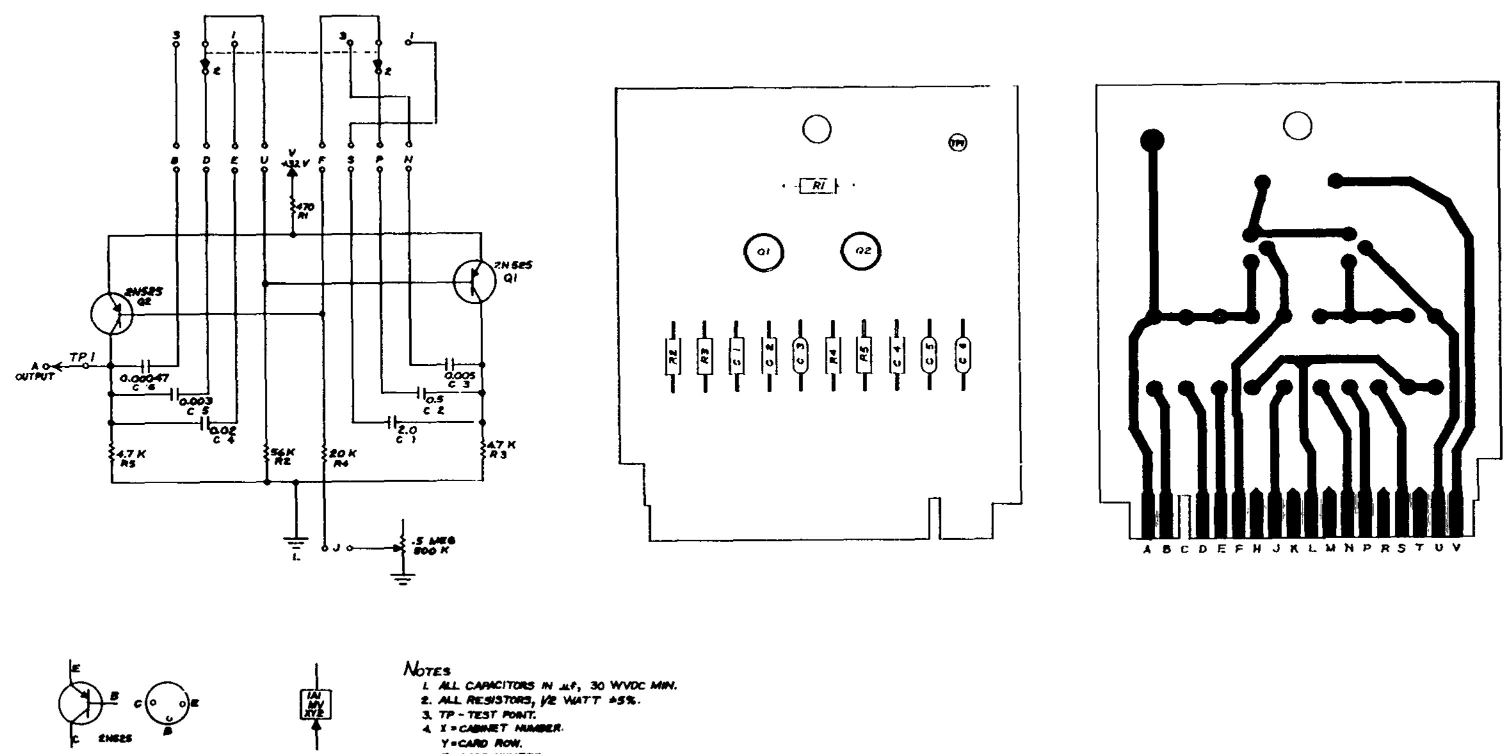
15,000 channels per second. These data were then punched on paper tape by the computer and checked for errors. These tests gave satisfactory results.

5.0 CONCLUSIONS

The development of this system has proved that data can be transmitted from the PWT 16-Ft Supersonic Tunnel to the ERA 1102 computer at a much higher speed than is presently being utilized. The scanner now operates at the extremely slow speed of 20 channels per second because of the requirement of punching a paper tape record of all data points. High-speed operation of the scanner can be efficiently utilized only by the addition of magnetic tape units, core storage, and a high-speed line printer to the present computer, or by the acquisition of a modern computer with these features.

DRAWINGS

LETTER	REVISION	DATE	BY	APPR.
A	PIV WAS 35V NOW 32V	7-10-61		



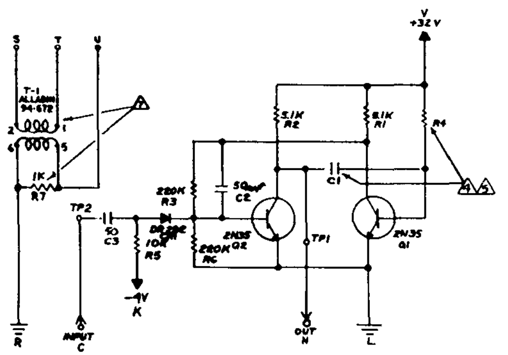
3201330A

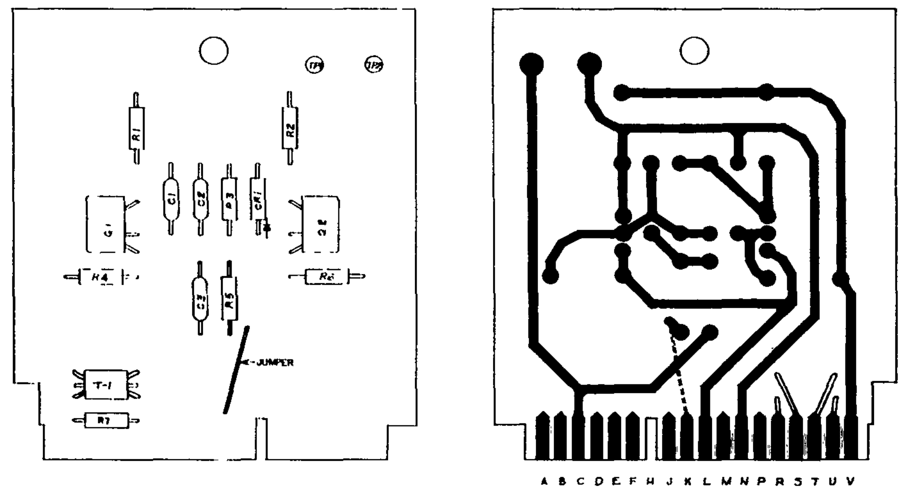
Notes
1. ALL CAPACITORS IN µf, 30 WVDC MIN.
2. ALL RESISTORS, 1/2 WATT ±5%.
3. TP - TEST POINT.
4. X = CABINET NUMBER.
Y = CARD ROW.
Z = CARD NUMBER.

DIODE SCANNER
FREE RUNNING MULTIVIBRATOR (20-20,000 CPS)
TYPE 1A1

3201330A

LETTER	REVISION	DATE	BY	APPD.
A	EXTENSIVE REVISION	11-11-60		
B	381 PINS WAS 3814	1-18-61		





3201333 B

Notes:

1. ALL RESISTORS 1/2 W ± 5%.
2. TP - TEST POINT
3. X = CABINET NUMBER.
   Y = CARD ROW.
   Z = CARD NUMBER.
4. ON CARD 4A1 R4 = 100K
   C1 = 11.0 μf.
5. ON CARD 4B1 R4 = 68K
   C1 = 1 μf.
6. 4A1 IN 2J14 HAS PIN V TO GROUND, PIN X TO -30VOLTS & PIN L THROUGH 680Ω 1/2 WATT RESISTOR TO -30 VOLTS ON 2C1 CARD LOCATED IN 2J12.
7. T1 & R7 ARE ON 4B1 CARD ONLY.

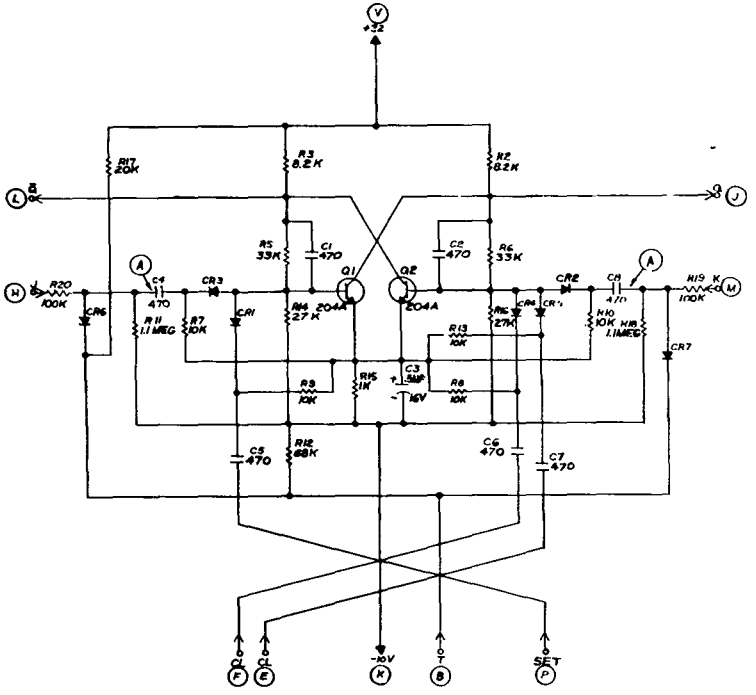
ARNOLD ENGINEERING DEVELOPMENT CENTER

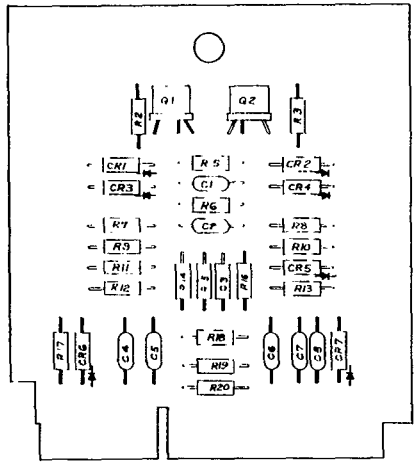
DIODE SCANNER
ONE SHOT
TYPE 4A1 (OR 4B1)

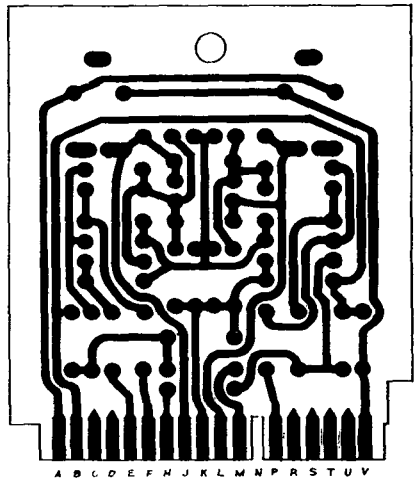
ARO, INC. TULLAHOMA, TENN.

3201333 B

LETTER	REVISION	DATE	BY	APPROVAL
A	C4 & C8 - 470 WAS 220	[illegible]	[illegible]	[illegible]
B	EXTENSIVE REVISION	7-18-61	[illegible]	[illegible]

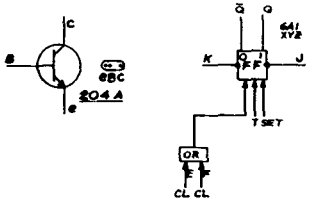






A B C D E F H J K L M N P R S T U V

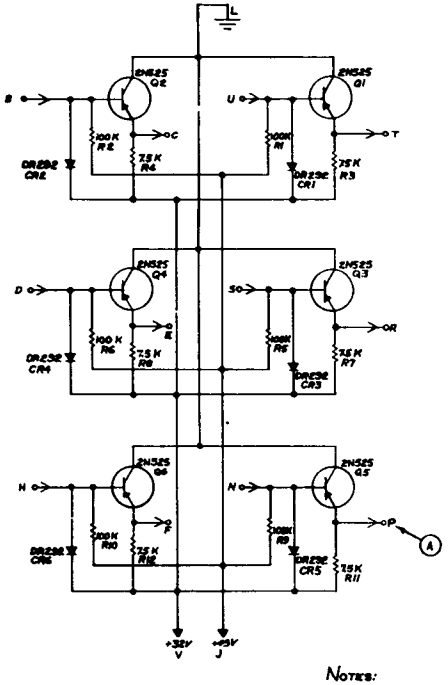
3201335

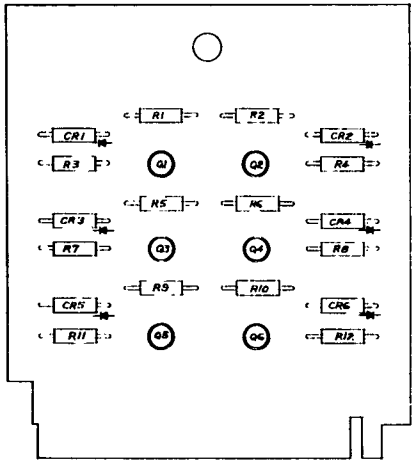


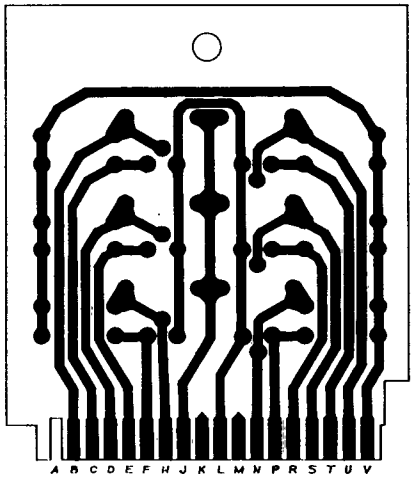
NOTES:
1. ALL DIODES TYPE DR 292.
2. ALL RESISTORS 1/2 W ±5%.
3. ALL CAPACITORS IN μμF UNLESS OTHERWISE SHOWN.
4. X = CABINET NUMBER
   Y = CARD ROW
   Z = CARD NUMBER

ARNOLD ENGINEERING DEVELOPMENT CENTER
DIODE SCANNER
FLIP FLOP
TYPE 6A1
ARO, INC.
TULLAHOMA, TENN.
TWICE SIZE
SANDERS
SCOTT
3201335 B

LETTER	REVISIONS	DATE	BY	APPROVED
A	TERMINAL POST P WAS D.	11-14-63	[illegible]	[illegible]
B	[illegible]	[illegible]	[illegible]	[illegible]

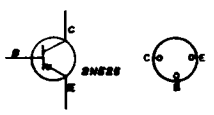






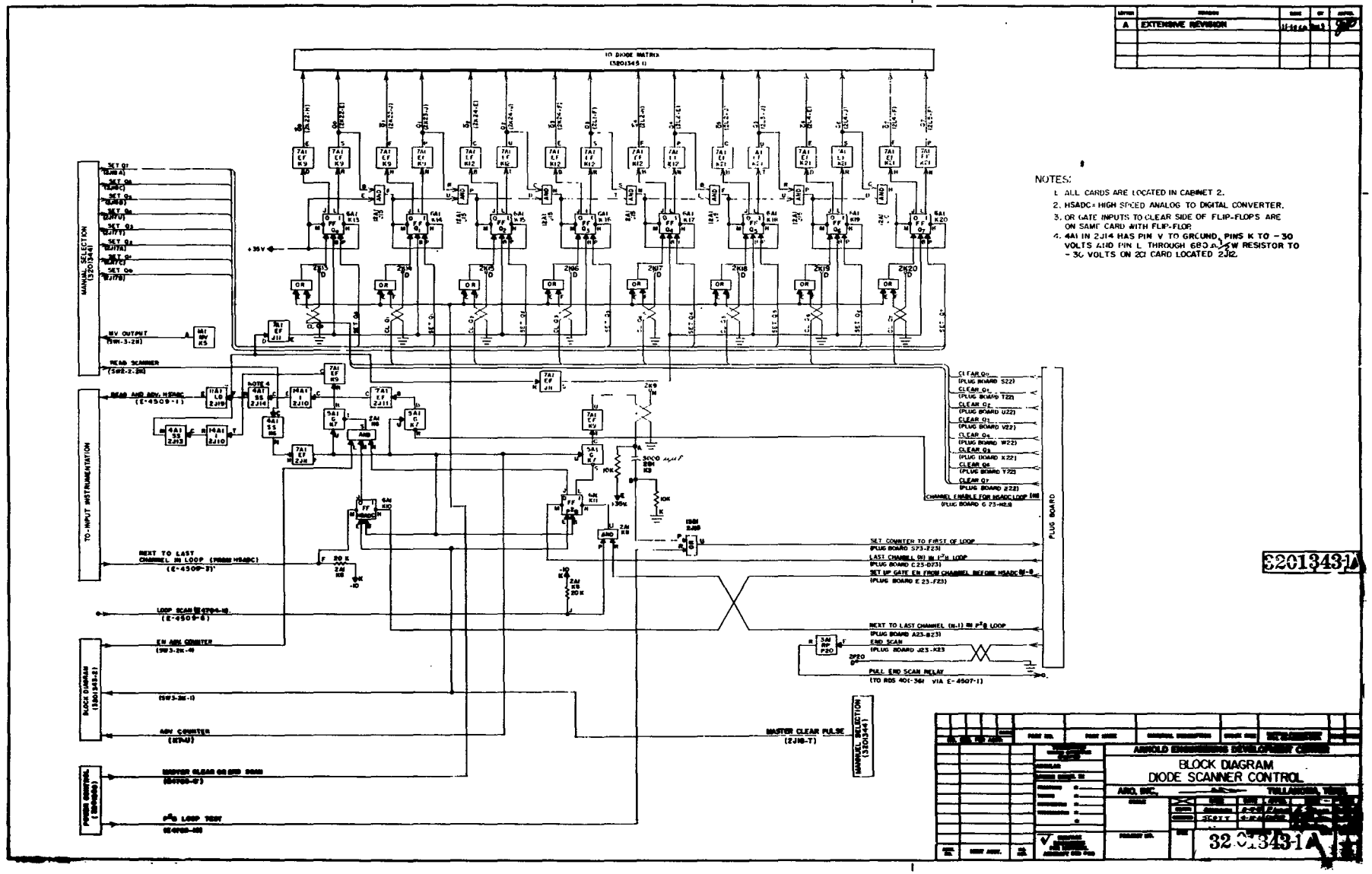
3201338 B

NOTES:
1. ALL RESISTORS ± 5% 1/2 W.
2. X = CABINET NUMBER.
   Y = CARD ROW.
   Z = CARD NUMBER.

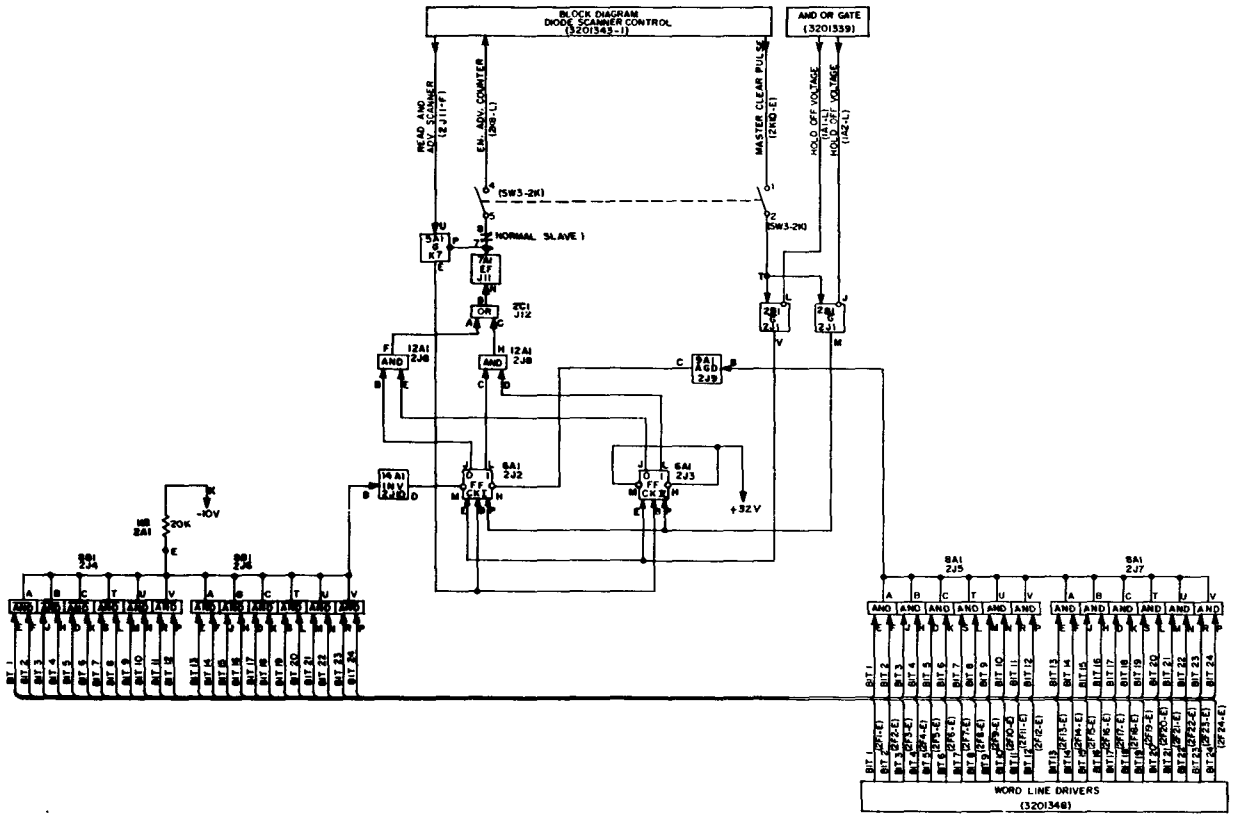


DIODE SCANNER
AND-OR-GATE DRIVER
TYPE SAJ

3201338 15


A EXTENSIVE REVISION
NOTES:
1. ALL CARDS ARE LOCATED IN CABINET 2.
2. HSADC = HIGH SPEED ANALOG TO DIGITAL CONVERTER.
3. OR GATE INPUTS TO CLEAR SIDE OF FLIP-FLOPS ARE ON SAME CARD WITH FLIP-FLOP.
4. 4AI IN 2J14 HAS PIN V TO GROUND, PINS K TO -30 VOLTS AND PIN L THROUGH 680Ω ½W RESISTOR TO -30 VOLTS ON 2D CARD LOCATED 2J12.
TO DIODE MATRIX
MANUAL SELECTION
TO-INPUT INSTRUMENTATION
BLOCK DIAGRAM
PLUG BOARD
MASTER CLEAR PULSE (2J18-T)
ARNOLD ENGINEERING DEVELOPMENT CENTER
BLOCK DIAGRAM
DIODE SCANNER CONTROL
ARO, INC.
32013431-1

LETTER	DESCRIPTION	DATE	BY	APPROV.
A	CHANGE: 2C1 WAS 2A1 & K8, 2A1 WAS J1, 2B1.	12-2-64	DC	
B	CHANGED FF CK X, +32 V was +36	7-26-68	RLC	



NOTE:

1. SW3-2K SHOWN IN OPEN (DOWN) CONDITION.

3201343-2

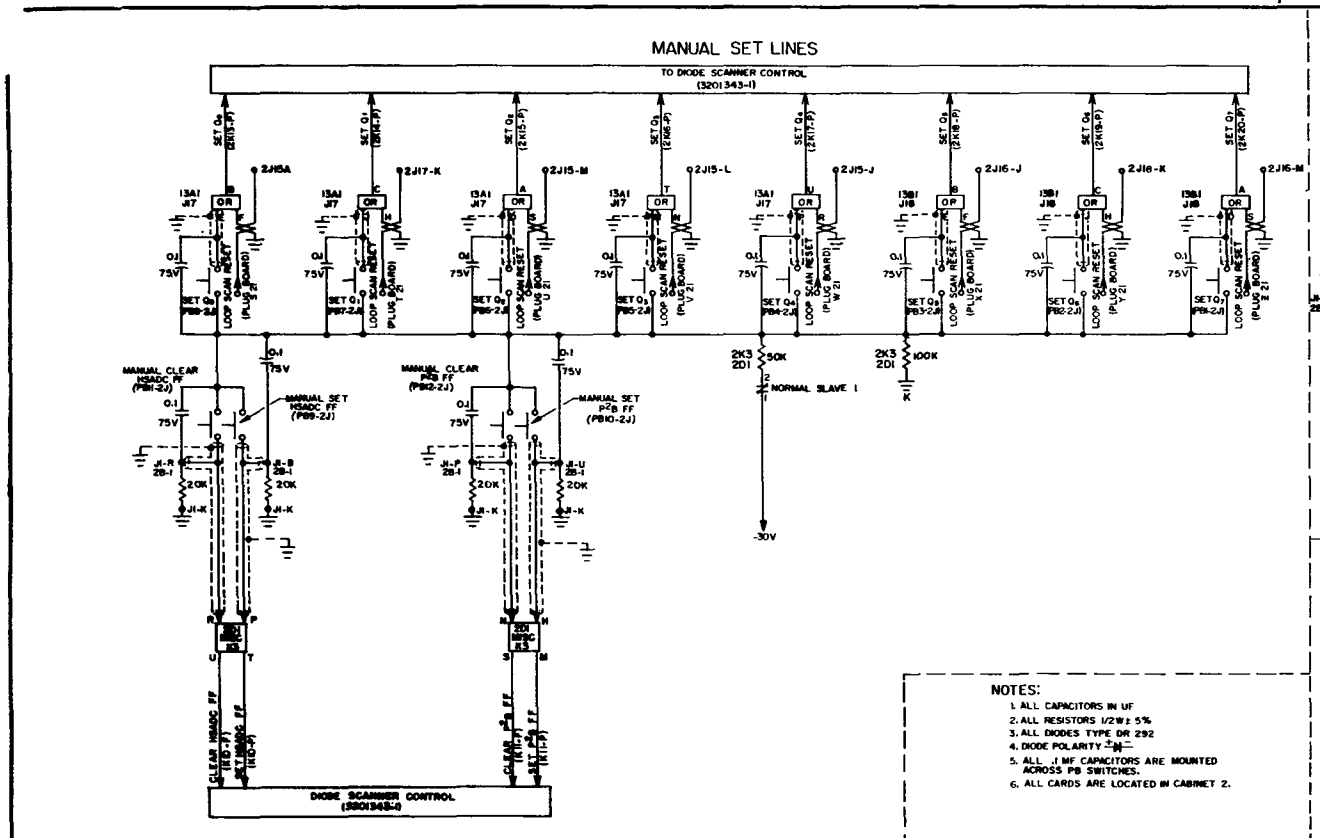
ARNOLD ENGINEERING DEVELOPMENT CENTER

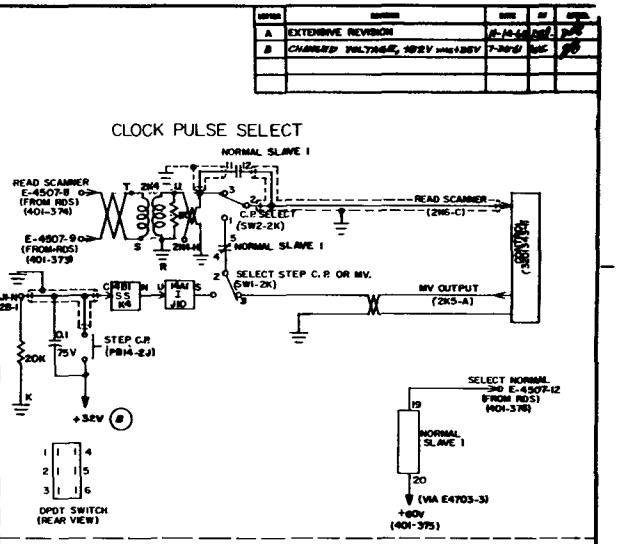
BLOCK DIAGRAM
DIODE SCANNER CONTROL
CHECKING CIRCUIT

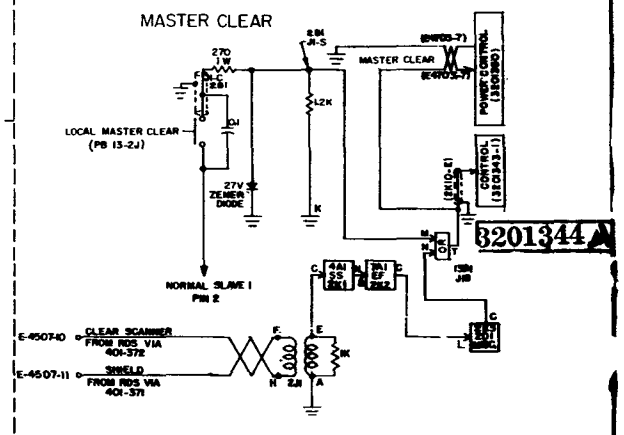
	SCOTT			

PROJECT NO. | DWG. | DRAWING NO. 3201343-2 | SIZE B | REV. B

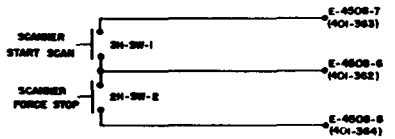
SHEET 1 OF 1







NOTES:
1. ALL CAPACITORS IN UF
2. ALL RESISTORS 1/2W ± 5%
3. ALL DIODES TYPE DR 292
4. DIODE POLARITY +|—
5. ALL .1 MF CAPACITORS ARE MOUNTED ACROSS PB SWITCHES.
6. ALL CARDS ARE LOCATED IN CABINET 2.

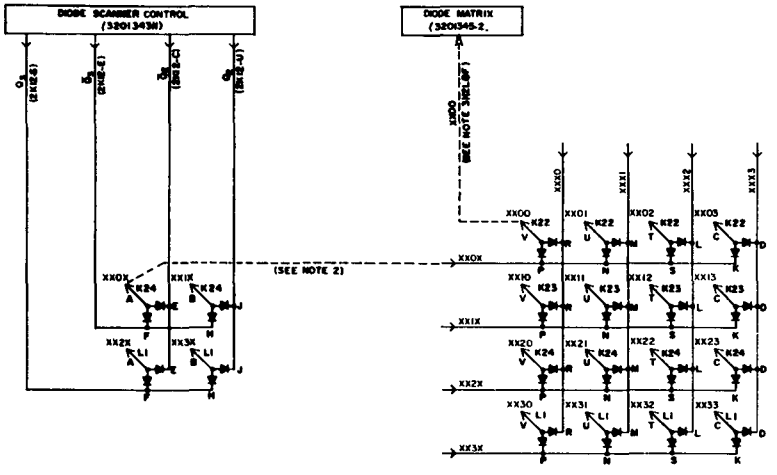


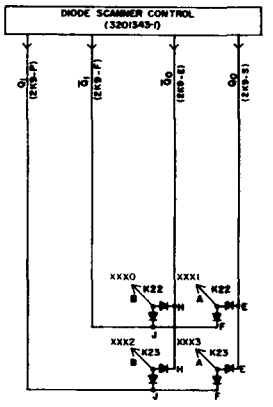
SCANNER START AND STOP CONTROL

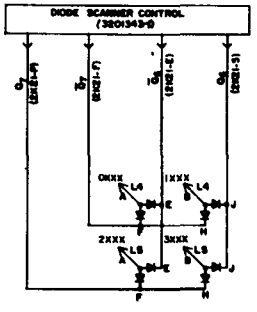
NUMBER	REVISIONS	DATE	BY	CHECKED
A	EXTENSIVE REVISION	[illegible]	[illegible]	[illegible]
B	CHANGED VOLTAGES, -32V and +28V	7-30-63	[illegible]	[illegible]

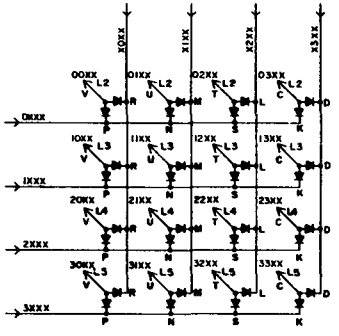
MANUAL SELECTION
DIODE SCANNER

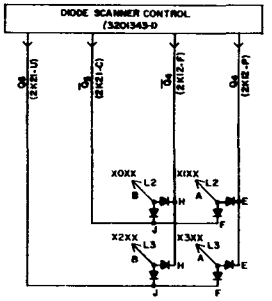
3201344 A











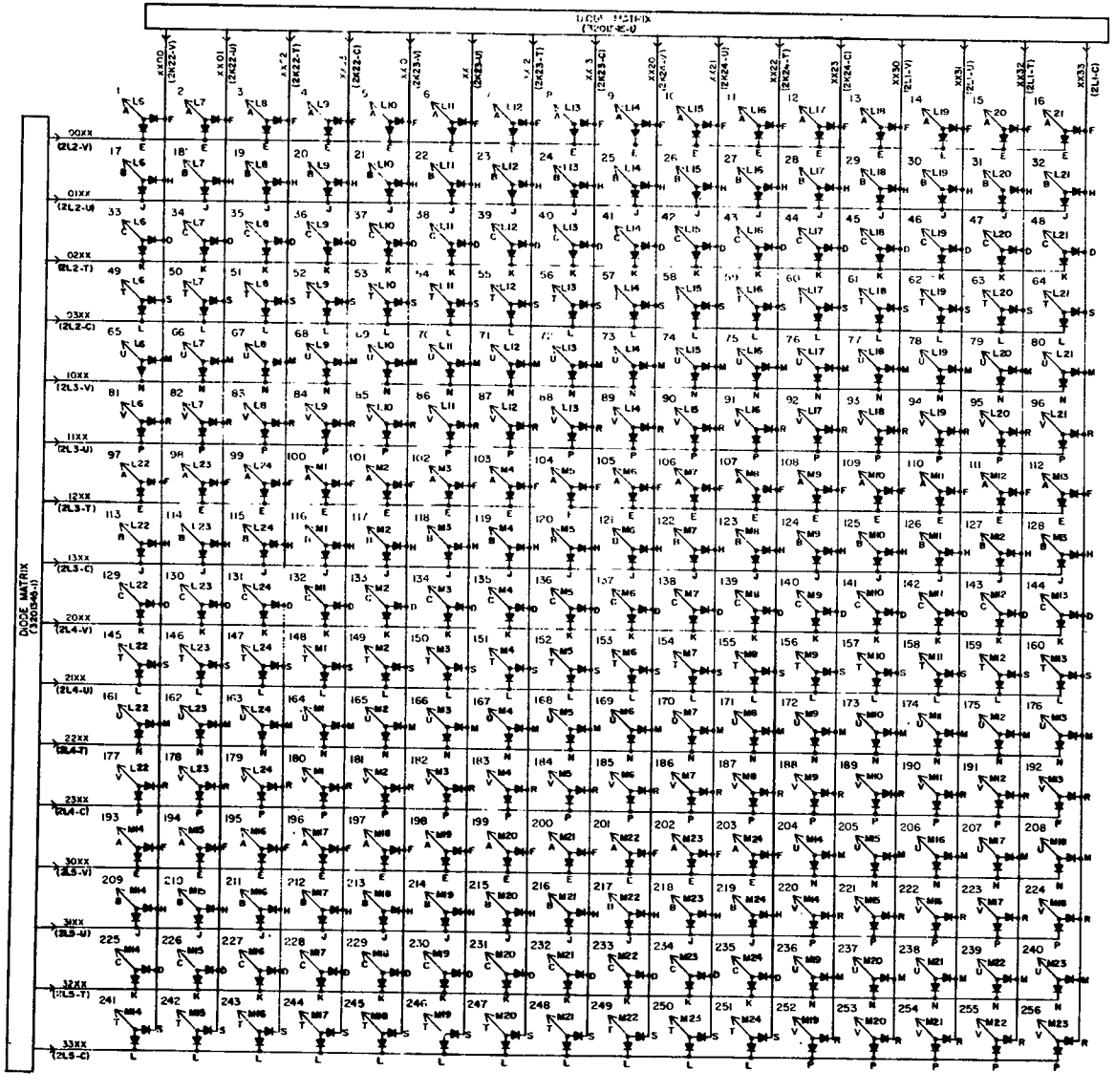
NOTES:

1. ALL CARDS ARE TYPE 8AI AND ARE LOCATED IN CABINET #2.
2. LINES CONTAINING THREE X'S AND ONE DIGIT ARE TERMINATED AT CORRESPONDING POINTS ON THIS DRAWING ie; XXOX (8K24-A) TO XXOX(8K22-F).
3. LINES CONTAINING TWO X'S AND TWO DIGITS GO TO CORRESPONDING POINTS ON 3201216-2 ie; XX00 (8K22-V) TO XX00 (2L6-F).
4. ALL DIODES ARE TYPE IN440 POLARIZED —10±

3201345-1

DIODE SCANNER
DIODE MATRIX SCHEMATIC

3201345-1



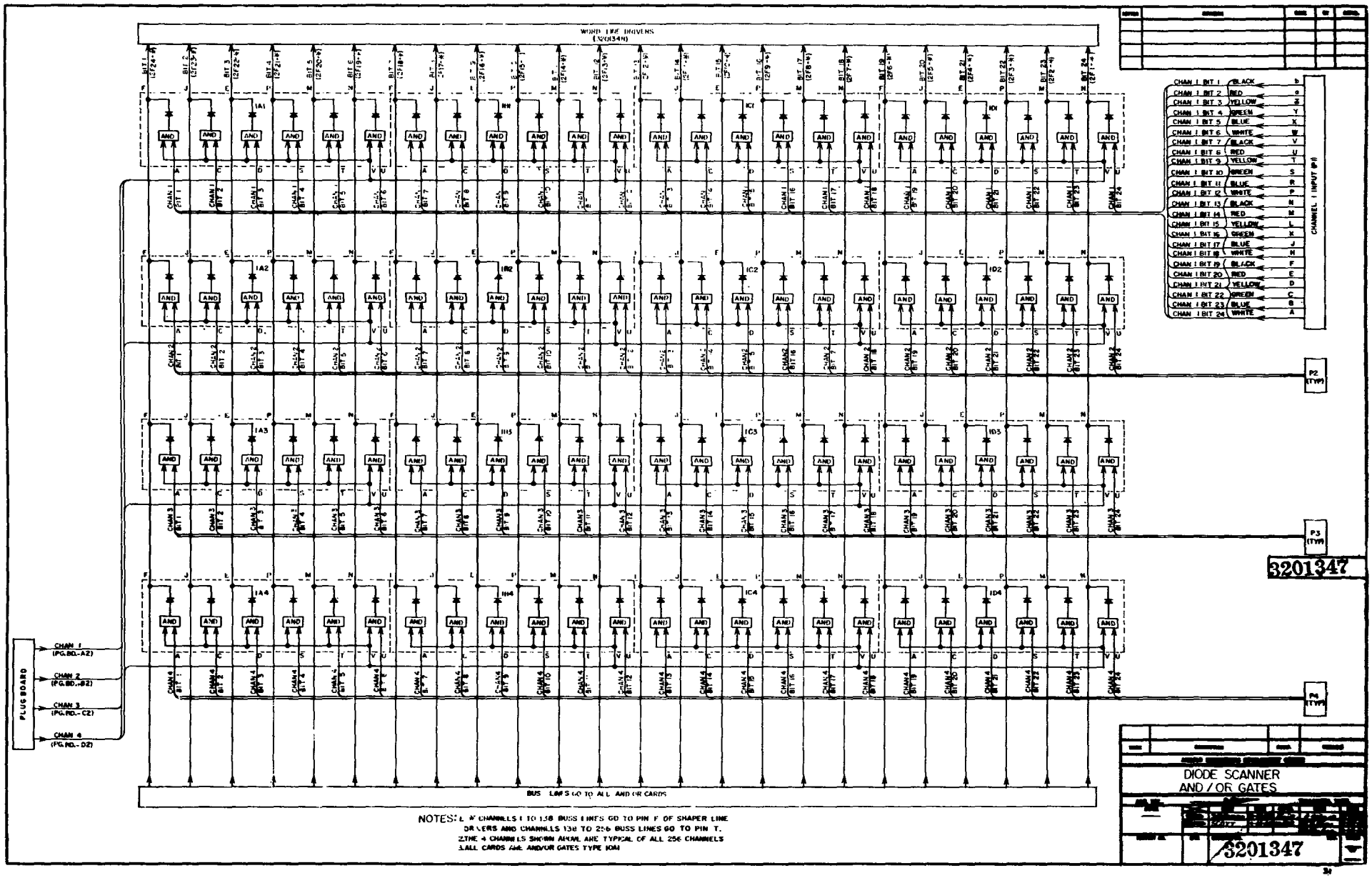
NOTES:

1. PINS U,N,M,RR,&V ON 2M24 ARE NOT USED.
2. ALL CARDS ARE TYPE 8AI AND ARE LOCATED IN CABINET 2.
3. ALL DIODE ARE TYPE IN440 POLARIZED

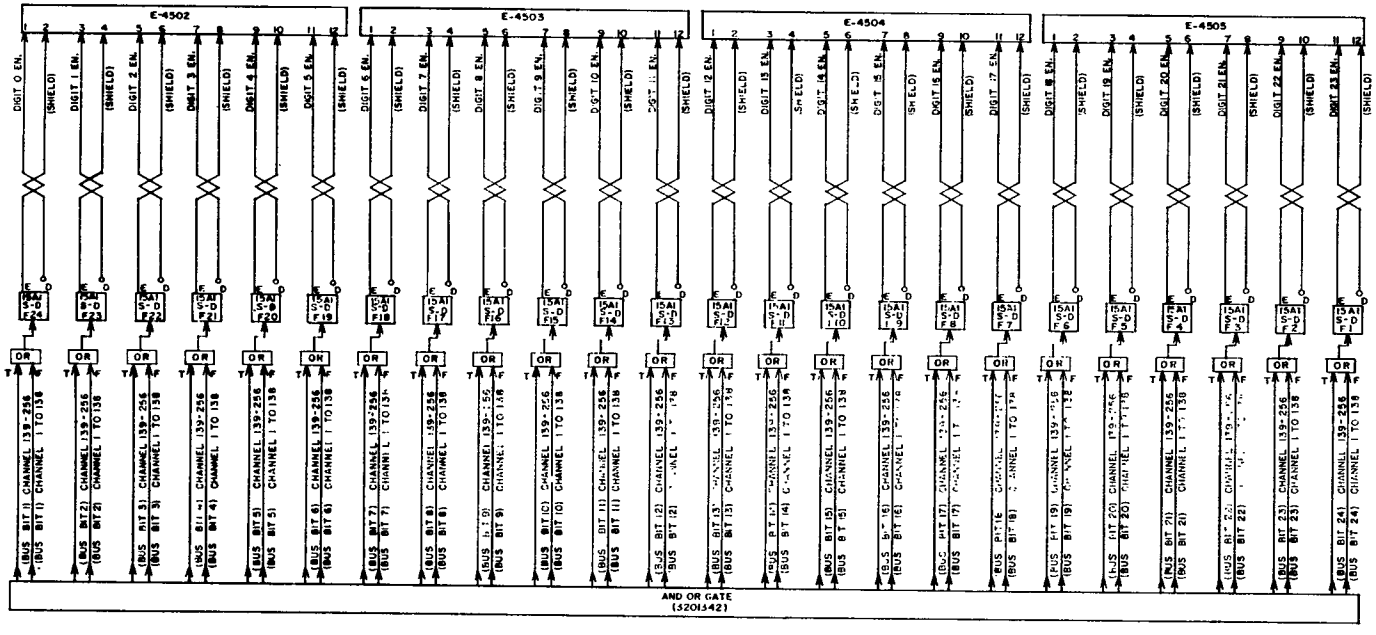
3201345-2

DIODE SCANNER
DIODE MATRIX SCHEMATIC

3201345-2



NOTES:
1. IF CHANNELS 1 TO 128 BUSS LINES GO TO PIN F OF SHAPER LINE DRIVERS AND CHANNELS 129 TO 256 BUSS LINES GO TO PIN T.
2. THE 4 CHANNELS SHOWN ABOVE ARE TYPICAL OF ALL 256 CHANNELS
3. ALL CARDS ARE AND/OR GATES TYPE 10A



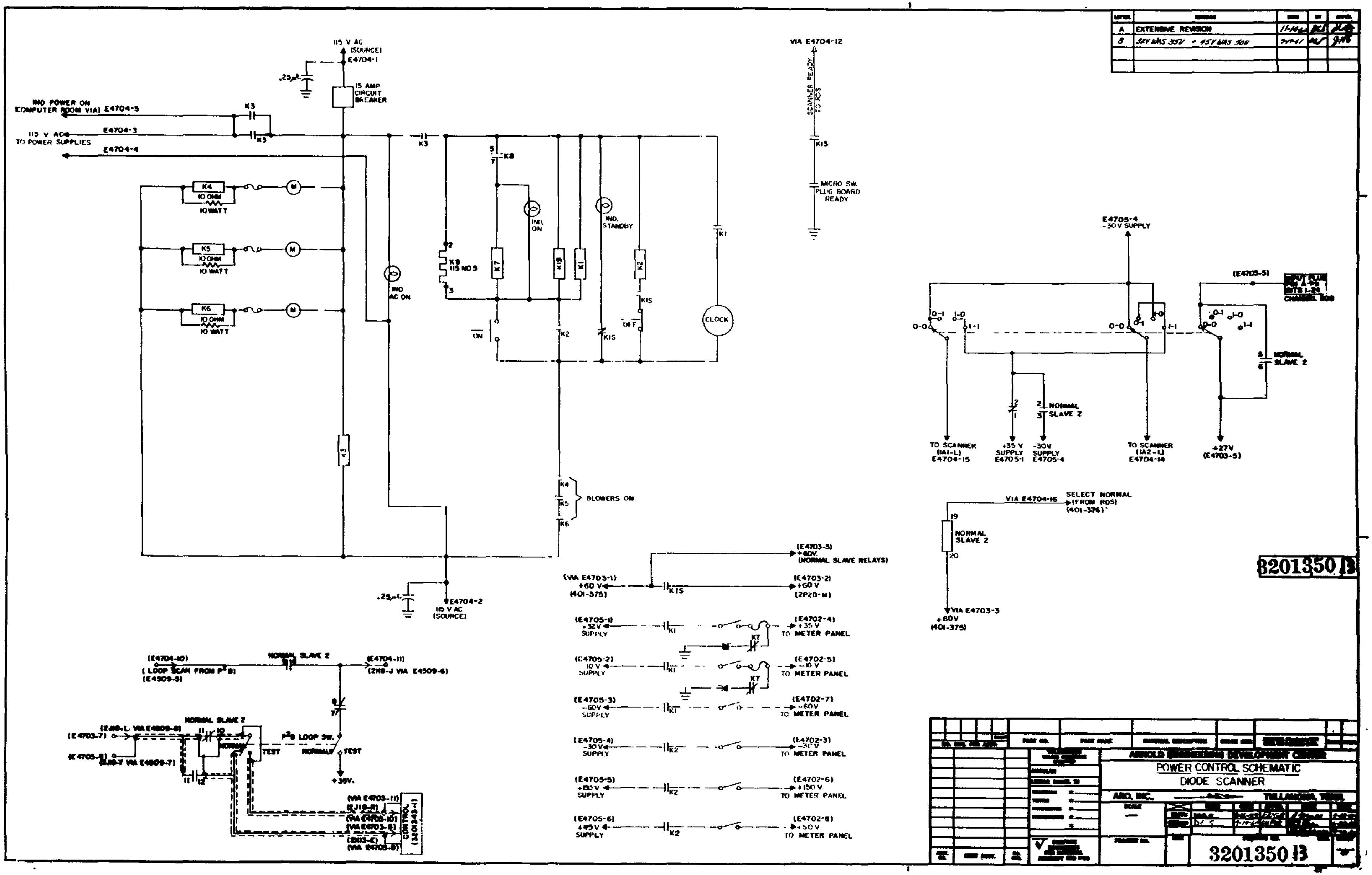
NOTES:

1. WLD = WORD-LINE DRIVERS.
2. ALL CARDS ARE LOCATED IN CABINET #2.

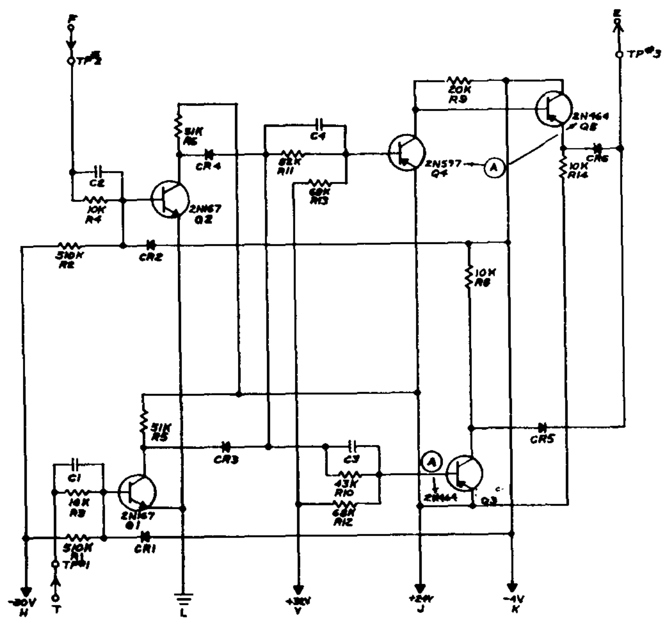
3201348

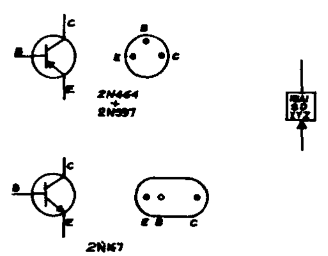
WORD LINE DRIVERS
DIODE SCANNER

3201348


A EXTENSIVE REVISION
B 32V WAS 35V + 45V WAS 50V
115 V AC (SOURCE) E4704-1
15 AMP CIRCUIT BREAKER
IND POWER ON (COMPUTER ROOM VIA) E4704-5
115 V AC TO POWER SUPPLIES E4704-3
E4704-4
K4 10 OHM 10 WATT
K5 10 OHM 10 WATT
K6 10 OHM 10 WATT
IND AC ON
K8 115 NO 5
IND. ON
ON
IND. STANDBY
OFF
CLOCK
BLOWERS ON
E4704-2 115 V AC (SOURCE)
VIA E4704-12
SCANNER READY TO RDS
MICRO SW. PLUG BOARD READY
E4705-4 -30V SUPPLY
(E4703-5)
NORMAL SLAVE 2
TO SCANNER (A1-L) E4704-15
+35 V SUPPLY E4705-1
-30V SUPPLY E4705-4
TO SCANNER (A2-L) E4704-14
+27V (E4703-5)
VIA E4704-16
SELECT NORMAL (FROM RDS) (401-376)
VIA E4703-3
+60V (401-375)
(E4703-3) +60V (NORMAL SLAVE RELAYS)
(VIA E4703-1) +60 V (401-375)
(E4703-2) +60 V (2P2D-M)
(E4705-1) +32V SUPPLY
(E4702-4) +35 V TO METER PANEL
(E4705-2) 10 V SUPPLY
(E4702-5) -10 V TO METER PANEL
(E4705-3) -60V SUPPLY
(E4702-7) -60V TO METER PANEL
(E4705-4) -30 V SUPPLY
(E4702-3) -30 V TO METER PANEL
(E4705-5) +150 V SUPPLY
(E4702-6) +150 V TO METER PANEL
(E4705-6) +45V SUPPLY
(E4702-8) +50 V TO METER PANEL
(E4704-10) (LOOP SCAN FROM P B) (E4509-5)
NORMAL SLAVE 2
(E4704-11) (2K8-J VIA E4509-6)
(E4703-7)
(E4703-8)
P B LOOP SW.
NORMAL TEST
+35V.
CONTROL (320134-1)
8201350 B
ARNOLD ENGINEERING DEVELOPMENT CENTER
POWER CONTROL SCHEMATIC
DIODE SCANNER
ARO, INC.
TULLAHOMA, TENN.
3201350 B

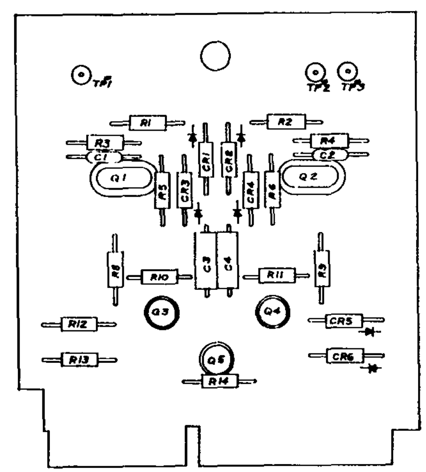
Rev.	Description	Date	By	Appr.
A	Q3 & Q5-2N464 WAS 2N525	11-11-[illegible]	[illegible]	[illegible]
	Q4-2N597: WAS 2N525			
B	EXTENSIVE REVISION	7-18-61	[illegible]	[illegible]

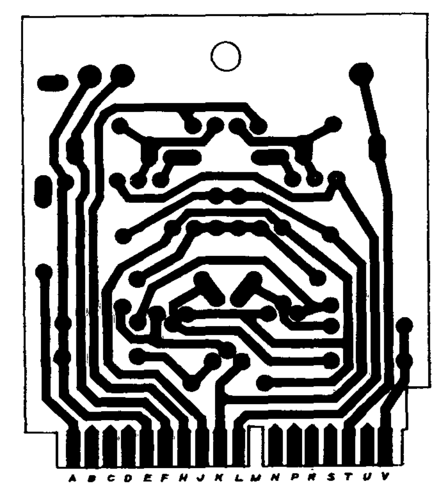




NOTES:

1. ALL RESISTORS 1/2 W ±5%.
2. ALL DIODES DR236.
3. ALL CAPACITORS 100μμf.
4. X=CABINET NUMBER
   Y=CARD ROW.
   Z=CARD NUMBER





3201351 B

[illegible]	PART NO.	PART NAME	MATERIAL DESCRIPTION	[illegible]	[illegible]

ARNOLD ENGINEERING DEVELOPMENT CENTER

DIODE SCANNER

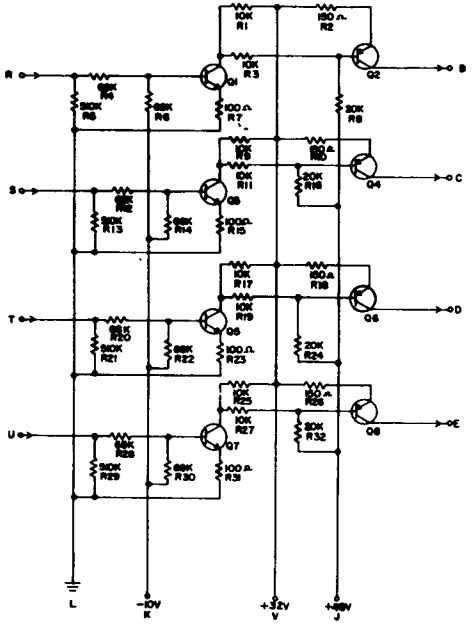
SHAPER LINE DRIVER
TYPE [illegible]

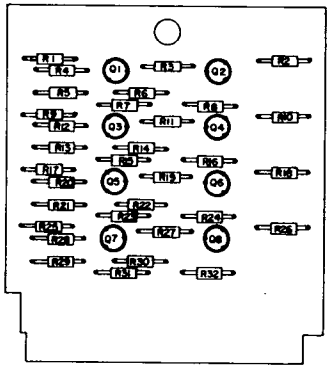
ARO, INC. — TULLAHOMA, TENN.

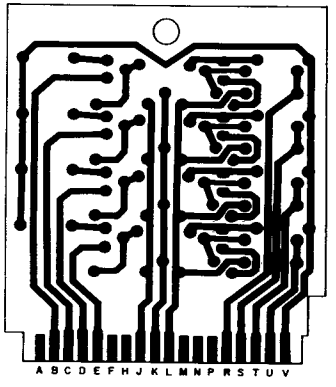
SCALE: TWICE SIZE

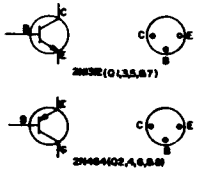
3201351 B

20









3201397

DIODE SCREEN
LAMP DRIVER
MAIN CARD TYPE

3201397

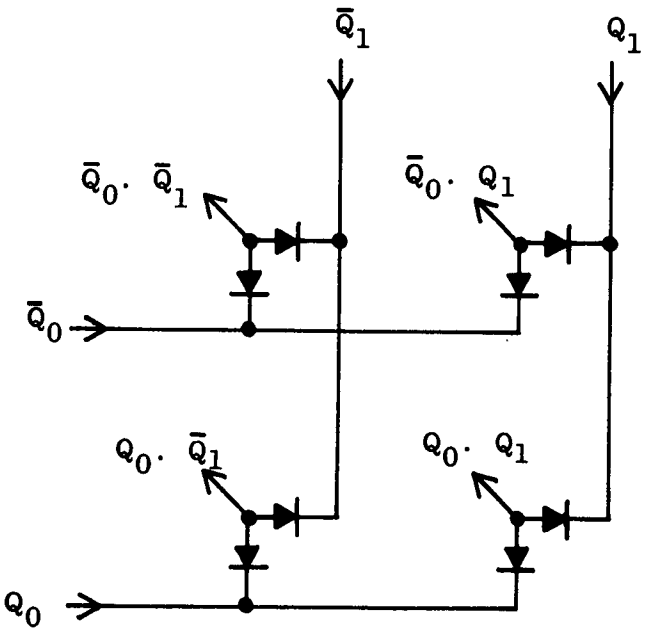


Fig. 1 2 x 2 Matrix

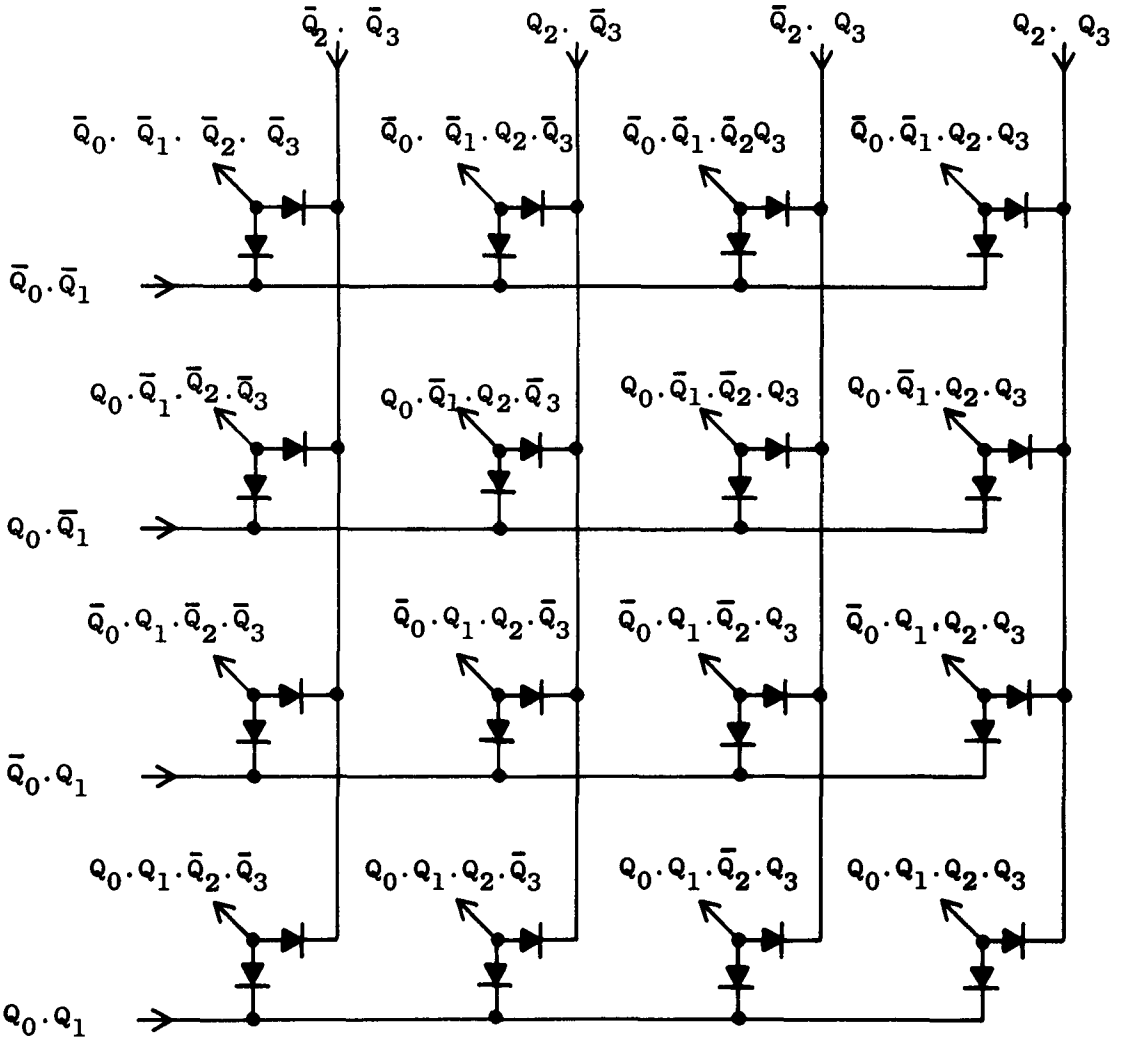


Fig. 2 4 x 4 Matrix

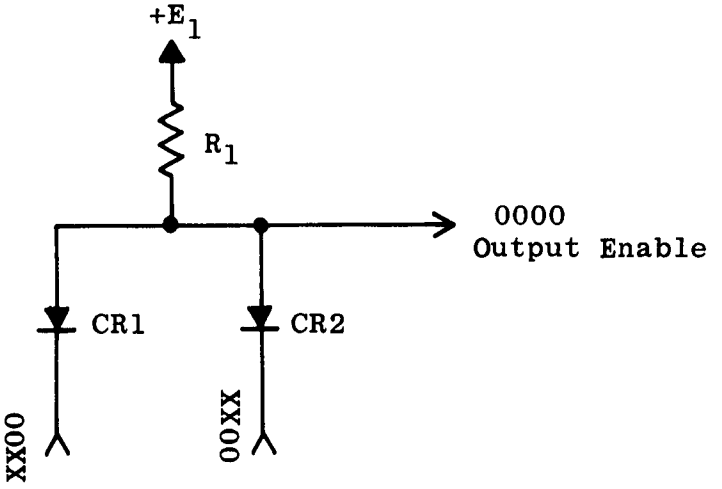


Fig. 3 Matrix Termination

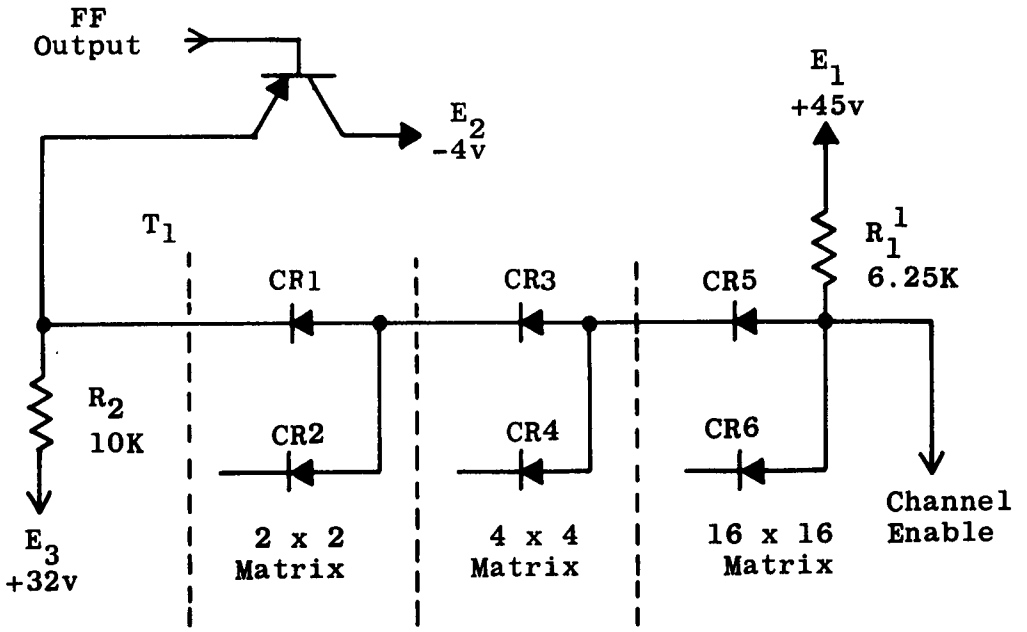


Fig. 4 Matrix Input

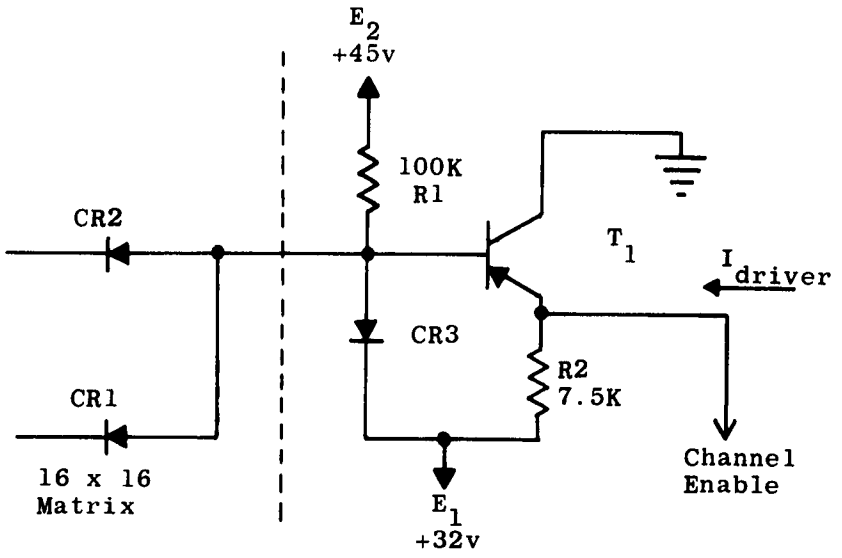


Fig. 5 Matrix Termination

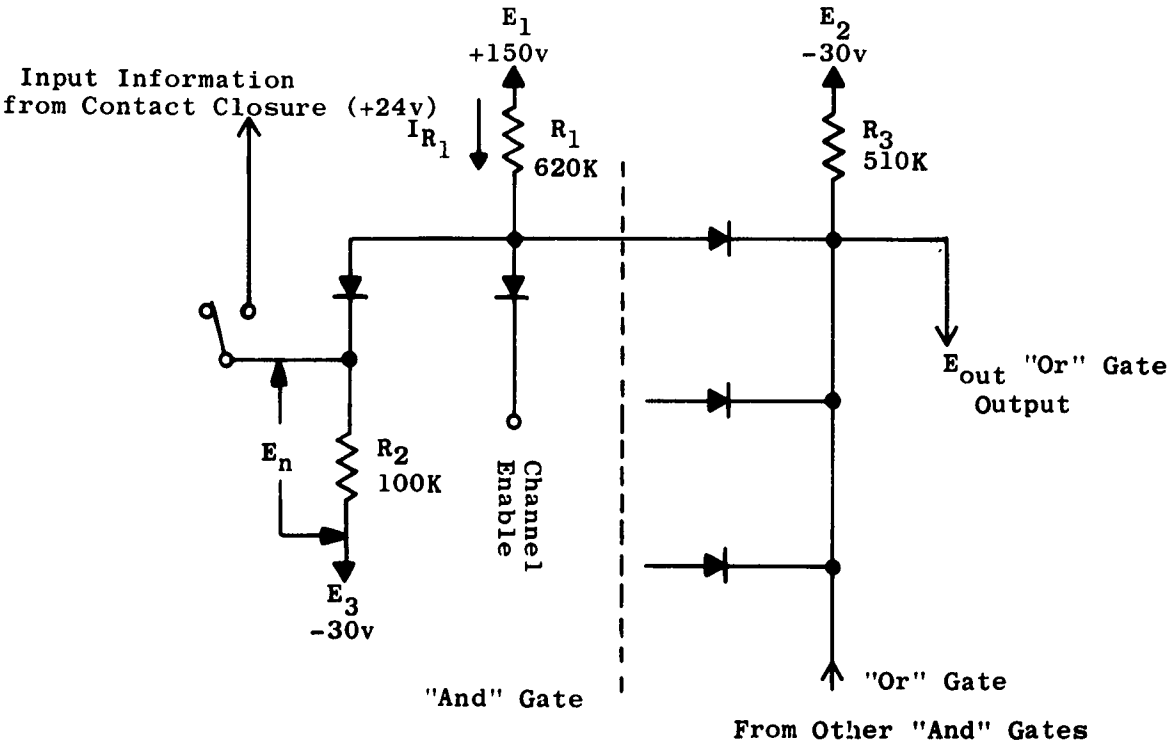


Fig. 6 "And-Or" Gate

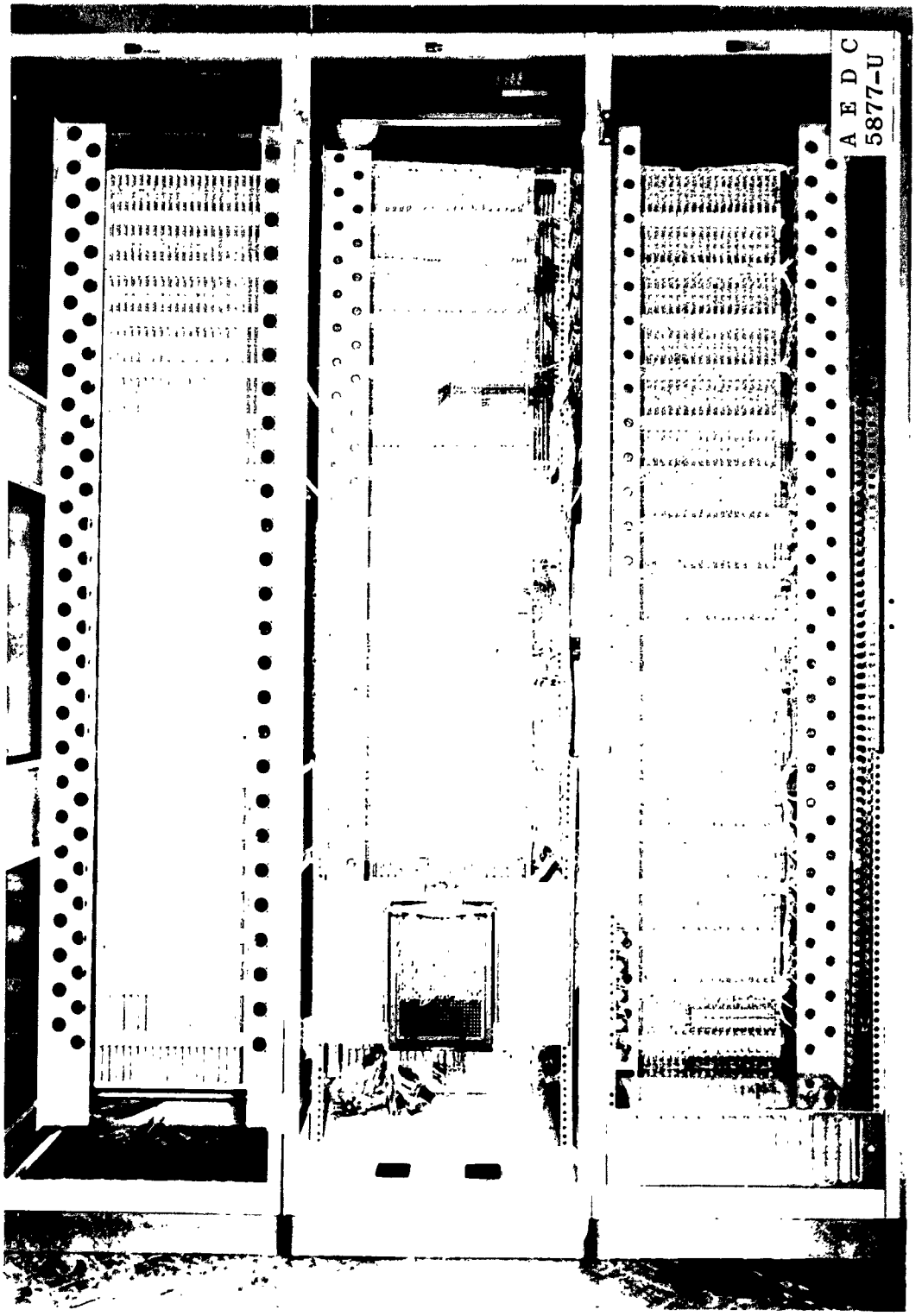


Fig. 7 Rear View of Unfinished Scanner

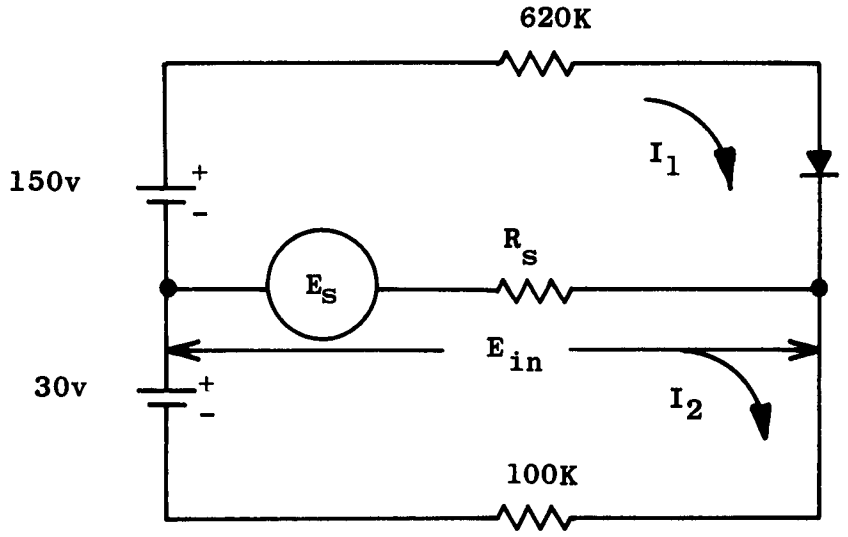


Fig. 8 Input Equivalent Circuit

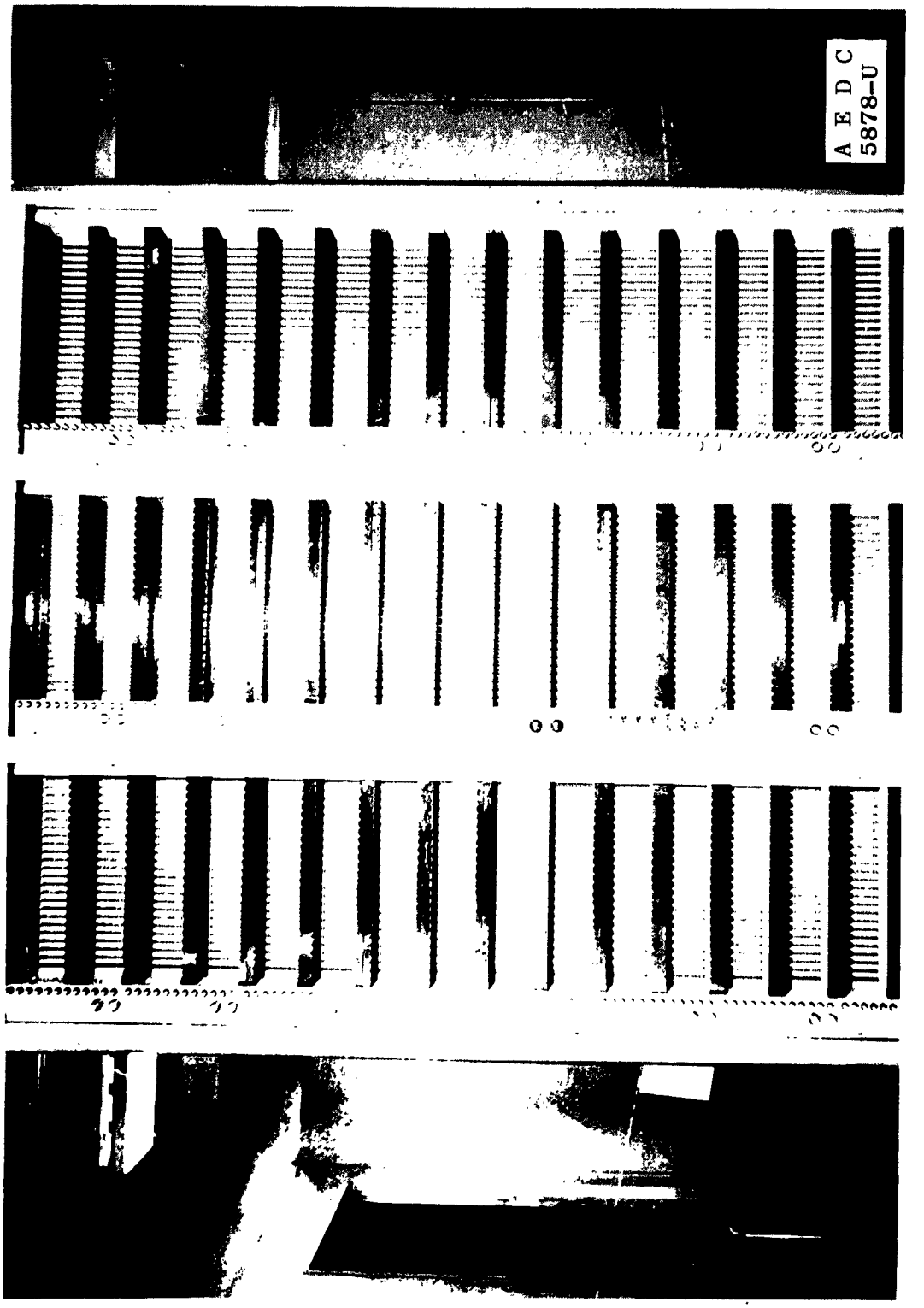


Fig. 9 Front View of Scanner without Circuit Cards

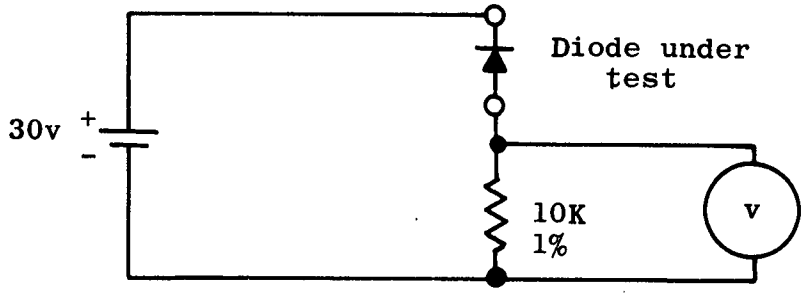


Fig. 10 Diode Testing Circuit

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6. Operation
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